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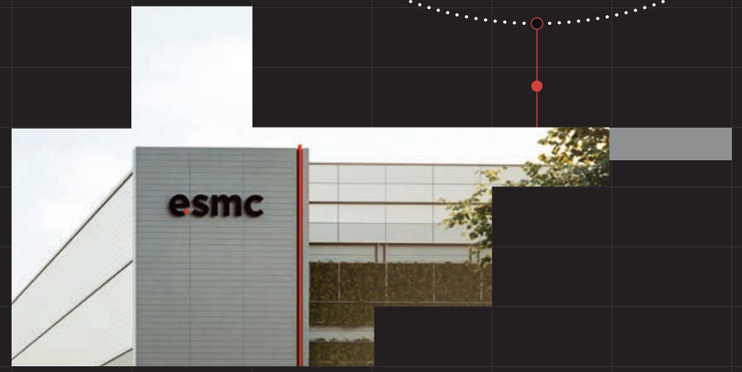

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Operational Highlights

TSMC manufactured 12,682 different products using 305 distinct technologies for 534 different customers.

5.1 Business Activities

5.1.1 Business Scope

As the founder and a leader of the dedicated semiconductor foundry segment, TSMC provides a full range of integrated semiconductor foundry services including leading advanced process and specialty technologies, advanced mask technologies, TSMC 3DFabric® advanced silicon stacking and packaging solutions, excellent manufacturing productivity and quality, as well as comprehensive design ecosystem support, to meet a growing variety of customer needs. The Company strives to provide unparalleled total value to its customers and views customer success as its own success. As a result, TSMC has gained customer trust from around the world and has experienced strong growth and success of its own.

TSMC made numerous technological advances in 2025:

Logic Technology

- A14 technology is the Company's next-generation, cutting-edge logic technology. A14 delivers full-node performance, power, and area (PPA) improvements through advanced dimensional scaling, setting a new benchmark for innovation. Optimized for high-performance computing (HPC), smartphone, and artificial intelligence (AI) applications, its development is progressing smoothly.
- TSMC A16™ technology features a nanosheet transistor structure with innovative backside power rail solution and provides greatly improved logic density and performance. It will further extend TSMC's technology leadership with even better PPA than N2P.
- 2nm (N2) technology development made excellent progress in both yield and performance improvement in 2025. N2 technology features TSMC's first generation of nanosheet transistor technology with full-node strides in performance and power consumption. Volume production started in 2025 as planned.
- 3nm fin field-effect transistor (FinFET) (N3) technology entered its fourth year of volume production in 2025 for customers' smartphone and HPC products.
- N3 Enhanced (N3E) technology, an enhanced version of N3 technology, continues to provide industry-leading advantages for both mobile communication and HPC applications. It entered its third year of volume production in 2025.
- N3P technology, an enhanced version of N3E technology, provides industry-leading advantages for both mobile communications and HPC applications. It entered its second year of volume production in 2025.
- N3 Compact (N3C) technology, building on N3P, offers compact cells, cost-effectiveness, and a simplified process. With backward-compatible design rules, N3C enables seamless IP reuse and minimal design effort. Customer tape-out was received in 2025 and volume production is expected in 2026.
- N3X technology, a process tailored for HPC applications, was introduced in 2023 and completed qualification in 2024 and started volume production in 2025.
- 4nm FinFET (N4) technology, an enhanced version of 5nm FinFET (N5) technology, entered its fourth year of volume production in 2025.
- N4P technology, with an additional performance boost over N4 technology, entered its third year of volume production in 2025.
- N4 Compact (N4C) technology features innovative process improvements that offer higher density components and simplified process flow compared to N4P technology. It received customer product tape-outs in 2025.
- N4X technology, introduced in 2021, was TSMC's first HPC-focused technology. It represents the ultimate performance and maximum clock frequencies in TSMC's 5nm family and entered its second year of volume production in 2025.
- N5 Plus (N5P) technology, a performance-enhanced version of 5nm technology (N5), entered its fifth year of volume production in 2025 for customers' smartphones and HPC products.
- 6nm FinFET (N6) technology, widely adopted for smartphones, HPC, and digital consumer electronics (DCE) products, entered its sixth year of volume production in 2025.
- N6e® Ultra-Low Power (ULP) technology service's process design kits (PDK) and ecosystem of low Vdd SRAM, ULL_ SRAM, and low Vdd standard cell libraries have been released and adopted by wearable applications. It entered its second year of volume production in 2025 with more comprehensive offerings.
- 7nm FinFET (N7) family technologies, widely used in customers' 5G and HPC products for several years, entered their fifth year of volume production for DCE and automotive products in 2025.
- N12e® technology service continued to be well received for a variety of product applications in 2025, including microcontroller unit (MCU), application processor (AP), memory controller, and IoT connectivity, and vision/voice AI products. This technology service offers more low Vdd and ultra-low leakage devices solutions for speed and power optimization.
- 22nm Ultra-Low Leakage (ULL) technology entered its seventh year of volume production in 2025 having been adopted in a wide range of applications, including wireless connectivity products such as Bluetooth and Wi-Fi for IoT, MCU, digital TV chips, and smartphones.

Specialty Technology

- N3A automotive technology, based on N3E technology, is TSMC's most advanced automotive grade process to date. TSMC introduced the N3 Auto Early (N3AE) program in 2023, providing automotive PDKs to support automotive customers in designing with the most advanced 3nm technology for automotive applications. N3A V1.0 PDK was released in 2025 and the technology completed automotive grade qualification and offered automotive design enablement platform (ADEP).
- N4 Auto Early program (N4AE), based on N4P platform, was in development for automotive grade technology in 2025 with full automotive process qualification targeted for the end of 2026.
- N4C radio frequency (N4C RF) technology, the next generation of N4P RF technology, is in development and is expected to be launched in 2026.
- 5nm FinFET automotive (N5A) technology has received multiple customer product tape-outs since 2023. Some products were prototyped, qualified for automotive applications, and successfully entered volume production utilizing TSMC's automotive service package (ASP) in 2025.
- Second-generation N6 RF (N6 RF+) technology development was completed and its V1.1 PDK was released in 2025.
- 12FFC+ RF technology process enhancements offer an advanced RF f_T/f_{MAX} corner model, ultra-thick metal (UTM) with aggressive metal width push, and extreme narrow-width high resistance offerings in 2025. The technology has entered its third year of volume production for customers' 4G and 5G cellular RF and IoT wireless connectivity products in 2025.
- 16FFC FinFET Compact (16FFC) RF Enhancement III technology is in development, with continuous improvement of 16FFC RF technology, is expected to be launched in 2026. 16FFC RF technology has received many customer tape-outs since 2021. Development of its enhanced version (Enhancement I/II) was completed in 2022 to support applications such as 28/39/47GHz mmWave RF front-end module and 77GHz/79GHz automotive radar.
- 16MRAM technology, TSMC's second generation of magnetoresistive random-access memory (MRAM) technology, passed automotive grade qualification in 2025, achieving <1ppm chip fail rate after one million cycles.
- N12e® RRAM technology service, TSMC's third generation of resistive random-access memory (RRAM) solution, features balanced cost and performance and passed consumer grade qualification for production in 2025.
- 22RRAM technology, TSMC's second generation of RRAM technology, passed the 100K-cycle qualification in 2025 for high-endurance product applications with various memory macro offerings.
- 28nm high voltage (HV) technology entered its second year of volume production for smartphone organic light-emitting diode (OLED) display applications in 2025.
- 40nm silicon on insulator (N40SOI) technology on 12-inch wafers, which provides industry-leading competitive advantages, entered its fourth year of volume production in 2025.
- 80nm HV technology for micro-OLED-on-Silicon display backplanes in augmented reality (AR)/virtual reality (VR) devices entered its fifth year of volume production in 2025. This technology offers extremely high density with over 3,000 pixels per inch (PPI), enhancing vision quality for near-eye applications.
- Advanced second-generation 40nm Bipolar-CMOS-DMOS (40BCD Gen-2) technology PDK was ready in 2025.
- Competitive 90nm BCD technology received multiple tape-outs and entered its second year of volume production in 2025. This technology is positioned as the next-generation platform for 0.18μm BCD technology for high digital content products such as charger and audio amplifier ICs. Additionally, the new continuous improvement plan (CIP) is underway, targeting server applications, and its PDK is scheduled to be ready in 2026.
- 0.13μm BCD technology continued to be optimized for the DCE and automotive markets. Its latest PDK was released in 2024.
- 0.18μm Gen-2 BCD technology was extended to 100V to support 48V power systems used in AI servers and electric vehicles (EVs). Its PDK was released in 2025. In addition, an automotive grade embedded non-volatile memory (eNVM) solution is targeted to be qualified in 2026 for 0.18μm Gen-3 BCD technology.
- CMOS image sensor (CIS) technology was further enhanced, enabling new capabilities of customers' CIS products. In 2025, TSMC helped customers ramp up advanced high dynamic range products for both smartphone and automotive markets.
- For silicon photonics technology, the Company continued development work on an innovative 3D photonics stacking technology – compact universal photonic engine (COUPE), which can integrate a silicon photonics chip and an electrical control chip into a single-chip photonic engine. This photonic engine can be co-packaged with an HPC chip to provide low-power and high-speed data transmission, achieving 200 gigabits per second (Gbps) with several customers in 2025. TSMC also continued working on co-packaged optics (CPO) solutions to reduce data transmission power consumption in data centers, targeting volume production in 2026.

TSMC 3DFabric® – TSMC Advanced 3D Silicon Stacking and Packaging Solutions

- TSMC-SoIC® Chip-on-Wafer (CoW) 3D vertical integration solution offers high-density interconnect for chiplet architecture for HPC products. 3nm system on integrated chip (SoIC) stacking technology successfully entered volume production in 2025.
- TSMC-COUPE™ technology service, leveraging the TSMC-SoIC® CoW stacking solution to integrate silicon photonics and electrical control chips for high-speed and low-power data transmission products, is on track for development, with volume production expected in 2026.
- CoWoS® advanced packaging service integrates multiple system-on-chip (SoC) chips and the high-bandwidth memory (HBM) stacks to enhance HPC products with superior compute power and memory bandwidth. CoWoS® with silicon interposer (CoWoS®-S) advanced packaging service features high interconnect routing density and embedded deep trench capacitor (eDTC) and has been in volume production for several years.
- CoWoS® with redistribution layer interposer (CoWoS®-R) advanced packaging service, featuring multiple redistribution layers (RDL) to enable product design simplicity, supports larger HPC products. This technology entered its third year of volume production in 2025.
- CoWoS®-L advanced packaging service enables larger HPC products by combining Chip on Wafer on Substrate with RDL-based interposer, higher density embedded local silicon interconnect (LSI), eDTC, and the integration of diverse embedded chips. This technology entered its second year of volume production in 2025 and is currently being adopted by multiple products featuring larger reticle interposer size, which are expected to start volume production in 2026.
- TSMC-SoW™ solution enables wafer-level heterogeneous integration for next-generation data center computing chips with better power efficiency, higher bandwidth, and greater chip density. The first-generation (logic only) technology entered its second year of volume production in 2025. The second generation, enabling the integration of logic and HBM, is currently on track in its development phase.
- Integrated Fan-Out Package-on-Package (InFO-PoP) technology enables advanced smartphone applications through the integration of SoC and dynamic random-access memory (DRAM). Products featuring backside RDL entered volume production in 2025.
- Fine pitch copper (Cu) bump technology for flip chip packaging on 2nm silicon successfully entered volume production in 2025.

5.1.2 Customer Applications

TSMC manufactured 12,682 different products for 534 customers in 2025. These chips were used across a broad spectrum of electronic applications, including artificial intelligence (AI) and high-performance computing servers, wired and wireless communication systems, automotive and industrial equipment, personal computers and peripherals and information appliances, as well as consumer electronics such as digital TVs, game consoles, digital cameras, AI-enabled IoT and wearables, and many others.

The rapid ongoing evolution of end products prompts customers to pursue product differentiation using TSMC's innovative technologies and services and, at the same time, spurs TSMC's own development of technology. As always, TSMC believes success depends on leading rather than following industry trends.

5.2 Technology Leadership

5.2.1 R&D Organization and Investment

The semiconductor industry is characterized by rapid technological change and the frequent introduction of new technologies to meet customer demand. To stay ahead of its competitors in the foundry service area, TSMC believes it must maintain its technology lead across the semiconductor industry.

In 2025, TSMC continued to invest in research and development, with total R&D expenditures amounting to 6.5% of revenue, a level that equals or exceeds the R&D investment of many other leading high-tech companies.

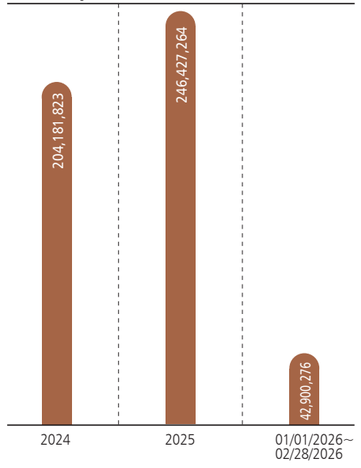
The Company continuously invests significant amounts in R&D to maintain its leading position in advanced process technologies. These efforts have allowed customers to access certain advanced process technologies, such as 7nm, 5nm and 3nm technology for volume production, ahead of competitors and many integrated device manufacturers. In addition, the Company is committed to developing more advanced process technologies to the 2nm level and below to sustain its leadership.

In 2025, as the development of 2nm technology progressed from the baseline consolidation to the yield enhancement stage, TSMC made good progress in the development of 16 Angstrom (A16) and 14 Angstrom (A14) technologies, which aim to further improve speed, power, density and cost. In addition, the Company's research efforts continued to push forward with exploratory studies for nodes beyond A14. The Company is also committed to investing in R&D for mature technologies to provide function-rich process capabilities to its customers.

TSMC's research and development efforts include both centralized activities and those undertaken by individual fabs. Centralized R&D focuses primarily on the development of new logic, SoC, derivatives and package/system-in-package (SIP) technologies, along with cost-effective 3D wafer-level system integration solutions, including TSMC-SoIC®, CoWoS®, TSMC-SoW™, and TSMC COUPE™. R&D at the fab level is mainly concentrated on improving and upgrading manufacturing process technologies.

TSMC has long maintained strong partnerships with several world-class research institutions, including the Semiconductor Research Corporation (SRC) in the U.S. and the Interuniversity Microelectronics Centre (IMEC) in Belgium. The Company continues to expand research collaboration with leading universities worldwide not only to advance semiconductor technologies but also to nurture human talent for the future.

R&D Expenditures Amount: NT$ thousands



5.2.2 R&D Accomplishments in 2025

Highlights

- 2nm Technology

In 2025, TSMC's 2nm technological development focused on baseline consolidation, yield enhancement, transistor and interconnect R/C performance improvement, and reliability qualification. During the year, customers completed IP design and qualification and performed more new tape-outs (NTOs). The Company also developed low resistance redistribution layer (RDL) and super high-performance metal-insulator-metal (MiM) capacitors to further boost performance for the 2nm process family.

- A16 Technology

TSMC's A16 technology development made significant progress in 2025 toward enhancing logic gate density and power efficiency to support HPC applications. Built upon 2nm process technology and design rules, A16 process technology adopts a backside power delivery network resulting in superior improvements in speed, power consumption, and density under the same design dimensions.

- A14 Technology

TSMC continued development of A14 in 2025 with good progress. The A14 platform offers significant improvements in speed, power, density and cost over 2nm technology. Development activities focused on manufacturing baseline process setup, yield learning, transistor and interconnect R/C performance. TSMC plans to continue full development of A14 in 2026.

- Lithography Technology

In 2025, TSMC remained dedicated to developing lithography technology. The focus included supporting 2nm technology for risk production and volume production and ensuring stable process advancement. Concurrently, the Company initiated the development and risk production preparation for TSMC A16™ process technology and continued with the development of A14 and more advanced technologies. The lithography R&D team made progress in enhancing process yield and performance, continuously improving the application efficiency of EUV scanners, reducing overlay errors, mitigating material defects, and developing and applying new mask pellicles and blanks. Furthermore, the Company began developing lithography technology for high numerical-aperture (High-NA) EUV scanners to support TSMC's continuous evolution in critical advanced process technologies.

• Mask Technology

In 2025, the TSMC R&D team advanced extra ultraviolet (EUV) mask technology for the A14 node and beyond. This was achieved by optimizing EUV blank materials, enhancing multi-beam writer resolution, and perfecting mask process conditions, thereby improving the uniformity of critical dimension, pattern fidelity, and overlay accuracy of curvilinear patterns. At the same time, by continuously developing advanced e-beam inspection and repair technologies, mask defects were reduced to further improve wafer yield and productivity. Future improvements will focus on the development of new blank materials and manufacturing technologies.

Integrated Interconnect and Packaging

3DFabric®, TSMC's fine pitch, chip-to-chip connection leveraging of wafer processes, consists of both wafer-level frontend and backend technologies. The Company's frontend technologies, or TSMC-SoIC®, enables leading-edge silicon for 3D silicon stacking. TSMC's advanced backend technologies includes CoWoS® advanced packaging service with chips placed onto pre-made RDLs and TSMC-SoW™ with system on wafer technology service that enables wafer-level heterogeneous integration. The Company's 3DFabric® technology service offers the ultimate flexibility in product design with integrated frontend and backend technologies to meet future computing systems integration scaling needs.

• 3DIC and TSMC-SoIC®

TSMC-SoIC® is an innovative wafer-level frontend 3DIC chip stacking platform with outstanding bonding density, interconnect bandwidth, power efficiency, and good stacking flexibility. It extends Moore's Law through system-level scaling with sustainable performance gains and corresponding cost benefits. SoIC integrated chips can be subsequently assembled by using conventional packages or TSMC's new 3DFabric® technology services, such as CoWoS® or TSMC-SoW™, for next generation HPC, AI and mobile applications. Several ongoing developments will allow the SoIC family to unleash more innovations, including the SoIC Gen-2 process that enables advanced SoC (N2 and beyond) compatibility and compact universal photonics engine (COUPE) to enable Si photonic solution. TSMC will continue to pursue SoIC technological improvements and co-optimize with the Company's advanced silicon technologies for further gains in transistor density, system PPA (power, performance, and area) and cost.

• CoWoS®

As the leading 2.5D technology, CoWoS® advanced packaging service has been experiencing strong growth due to surging AI demand since 2023. CoWoS®-L at 3.5-reticle size has been in production since 2024 and the 5.5-reticle size CoWoS®-L will finish the qualification in 2026 to meet higher performance goal in a package. The further development of the 9.5-reticle size CoWoS®-L is also making good progress. In parallel, CoWoS® Co-packaged optics (CPO) for ultra-high-end network switch is under development to integrate interposer-based CoW module and COUPE-based optical IO's into one package to achieve higher data bandwidth and reduce system power consumption.

• TSMC-SoW™

System-on-wafer technology provides wafer-level heterogeneous integration for data center computing chips, leading to higher chip density, improved power efficiency and increased bandwidth. The first generation, focusing solely on logic, began volume production in 2024. A second generation, which will integrate logic with high bandwidth memory (HBM), is currently under development.

• Advanced Interconnect

TSMC is developing state-of-the-art technologies for back end of line (BEOL) interconnects to meet the demand for chips with faster speeds and lower power consumption. In 2025, the Company developed a novel patterning approach and interconnect structures to enhance chip performance. Additionally, significant progress was made in novel material developments leading to a reduction in both wire resistance and capacitance. These innovations enable TSMC customers to deliver more compelling and competitive products.

Corporate Research

TSMC corporate research is a consistent leader in low-dimensional transistor exploration, innovating both devices and materials to achieve higher performance and lower power consumption for extremely scaled logic transistors. At the 2025 Symposium on VLSI Technology and Circuits (Symp. VLSI), TSMC showcased a carbon nanotube (CNT) nanosheet (NS) PFET that demonstrated record performance (I_{MAX} = 0.9 mA/μm) and remarkably low leakage (I_{MIN} of 20 pA/μm) at -0.5V V_{DS}. Furthermore, at the 2025 IEEE International Electron Devices Meeting (IEDM), TSMC presented significant advancements in 2D transition metal dichalcogenide (TMD) channel transistors. This research focused on three key areas: process integration to enhance the mechanical strength of the nanosheet (NS) channel, innovative contact engineering utilizing atomic layer deposition (ALD) epitaxial contact metal and phosphorous doping, and optimized dielectric materials. These collective efforts resulted in a 1.6X improvement in carrier mobility.

TSMC also continues its research into emerging high-density, non-volatile memory for AI and HPC applications. At the 2025 IEDM, the Company demonstrated a novel Type-C spin-orbit torque MRAM (SOT-MRAM) that featured for the first time a circular-shaped magnetic tunnel junction (MTJ) with built-in magnetic anisotropy (MA). This Type-C SOT-MRAM operates field-free while maintaining strong data retention and excellent performance. Furthermore, the Type-C device offers a 48% reduction in cell size and a 25% decrease in switching current, presenting a highly compelling solution for emerging applications that demand cost-effective, high-performance non-volatile memories.

Intra-chip thermal dissipation has become a critical issue for 3D integration with CMOS technology, given its higher power density and poorer heat dissipation. At the 2025 IEDM, TSMC demonstrated aluminum nitride (AlN) films as a promising and scalable thermal material for 3D ICs. Sub-500 nm thick polycrystalline AlN films achieved exceptionally high cross-plane and in-plane thermal conductivities, reaching up to 100 $Wm^{-1}K^{-1}$ and 30 $Wm^{-1}K^{-1}$, respectively.

TSMC continues to advance the frontier of hardware accelerators for AI and HPC applications. In a March 2025 Nature article, TSMC presented a mixed-precision, heterogeneous resistive random-access memory (RRAM) and static random-access memory (SRAM) compute-in-memory (CIM) AI edge processor. This work demonstrated state-of-the-art computational energy efficiency with minimal accuracy degradation. Furthermore, at the 2025 International Solid-State Circuits Conference (ISSCC), TSMC also presented a 16nm microscaling multi-mode gain-cell compute-in-memory macro. This macro was the first of its kind to support microscaling, integer, and floating-point formats, achieving the highest MX-MAC energy efficiency.

Specialty Technologies

TSMC offers a broad array of specialty technologies to address a wide range of applications:

• Mixed Signal/Radio Frequency (MS/RF)

In 2025, the semiconductor landscape saw a clear divergence between cutting-edge logic and premium, high-performance "workhorse" nodes. While 2nm and 3nm nodes drove flagship smartphone SoCs and the newest AI accelerators, the 4nm and 6nm node platforms solidified their roles as critical foundations for wireless cellular, networking, IoT, and HPC interconnects. The intersection of Edge AI and MS/RF technologies is driven by advanced semiconductor nodes, specifically 4nm and 6nm, to achieve high performance with ultra-low power consumption.

TSMC's MS/RF technologies are built upon product-proven logic process with comprehensive SPICE model and PDK support. The 4nm and 6nm RF technologies enable high-speed wireless connectivity for Edge AI applications. New low flicker noise devices at 4nm have been developed to meet challenging signal-to-noise ratio (SNR) specs. RF technology at 16nm is being optimized for mmWave auto radar application. TSMC will continue to refine its MS and RF technology offerings to enable customer innovations and accelerate product success.

• Power IC/Bipolar-CMOS-DMOS (BCD)

Due to the widespread adoption of Edge AI computing, the prerequisites for power management ICs (PMICs) in mobile devices have become increasingly stringent, requiring not only higher power density and superior energy efficiency but also extreme miniaturization. To meet this challenge, TSMC has successfully developed and launched two generations of industry-leading BCD (bipolar-CMOS-DMOS) technology platforms. In 2025, TSMC released a new 5V device process design kit (PDK) based on 55nm BCD technology, providing strong support for customers in designing high-performance, small-sized PMICs. Also in 2025, the Company began volume production of its second-generation 40nm ultra-low power (ULP) BCD process chips and developed technology entering the reliability verification stage to push the operating voltage to 45V, greatly extending the application range of the 40nm BCD process.

• Micro-Electromechanical Systems (MEMS)

In 2025, TSMC's PiezoMEMS platform technology was validated for its application in cooling HPC AI-related devices, effectively reducing the operating temperature of high-frequency computing chips. Furthermore, the next generation of high-voltage capacitive micromachined ultrasonic transducers (CMUT) was successfully validated for reliability. Future plans include developing applications such as wearable ultrasonic sensing technology.

Display Drivers

In 2025, TSMC completed N16HV platform reliability qualification and verified customer test-chip yield. The Company will begin the production yield validation stage in 2026. Additionally, to maintain the leading position in the field of high-voltage panel driver technology, TSMC began developing an N16HVP process with higher performance of HV/MV devices and lower power of logic devices, to help customers design more competitive OLED display driver ICs. Validation of customer test-chip yield is expected to start in 2026.

- **Complementary Metal-Oxide-Semiconductor (CMOS) Image Sensors**

TSMC achieved several key accomplishments in this area in 2025. For mobile applications, the Company developed a 3D-MiM (Gen-1) embedded lateral overflow integration capacitor (LOFIC) pixel, which was implemented in high-end smartphones, exhibiting a significant dynamic range improvement from 90dB to 110dB. Furthermore, a newly developed Gen-3 3D-MiM storage capacitor, offering a 12X capacitance boost compared to Gen-1, passed process qualification and mass production is scheduled for 2026. In advanced small pixel development, the world's smallest 0.43μm pitch quad photodiode CMOS image sensor, utilizing 3-wafer stacking and dual-backside deep trench isolation (dual-BDTI) technologies, was successfully demonstrated and introduced by TSMC at the 2025 IEDM. In parallel, the Company developed another low-cost process solution for advanced pixels, using dual-BDTI in a conventional 2-wafer stacked pixel in a 0.6μm-pitch pixel, achieving 10Ke- FWC while maintaining a significantly low dark current of 1e-/s at 60C. For photodetectors TSMC is developing a novel avalanched photodiode (APD) with a 7μm pixel pitch for Optical I/O in AI applications. This APD has already met industry requirements by achieving >2GHz operation with very low power consumption. Also, the Company made significant progress on Ge/Si heterogeneous SPADs (single-photon avalanche diodes), including an approximate tenfold reduction in dark count rate (DCR) and improved performance uniformity. This achievement was also presented at the 2025 IEDM.

- **Emerging Memory/Memory WoW Stacking Technology**

The Company reached several major milestones in emerging memory technologies in 2025. TSMC offered RRAM as a low-cost embedded non-volatile memory (NVM) solution for the price sensitive IoT market. The Company's 40nm, 28nm and 22nm nodes entered volume production and completed the technical qualification of 12nm consumer-grade RRAM, the 12nm automotive grade qualification is currently underway while 6nm node also entered development stage.

TSMC is firmly committed to developing MRAM technology, which performs very high-speed read/write operations with endurance in excess of a million read/write cycles, supports solder reflow, and has excellent high-temperature data retention. In 2025, TSMC successfully completed the qualification of 16nm automotive-grade MRAM and made this product available to meet customer requirements for high-specification memory. To address future market demand, TSMC is simultaneously developing 12nm automotive-grade MRAM and 5nm high-speed MRAM, aiming to support new applications in diverse fields such as automotive electronics, consumer electronics, data centers and communication equipment, industrial applications, and edge AI.

In 2025, the Company continued to develop wafer stacking (WoW) technology, creating a heterogeneous process platform for logic wafers and dynamic random-access memory. TSMC made good progress in the development of 55nm, 6nm, and 3nm logic wafers with single memory wafer stacking process technology. 55nm was the first to enter production with stable yields. TSMC will extend WoW technology to advanced logic wafers (6nm, 3nm) bonded with multi-wafer memory stacking to enable faster computing capabilities and higher memory bandwidth. WoW is suitable for AI chips and data center needs and can also be used in mobile phone chips and mining chips. This new memory architecture is compatible with advanced packaging technology, which is expected to satisfy a wide range of application needs and shorten product development times.

5.2.3 Technology Platform

TSMC provides customers with advanced technology platforms that include the comprehensive infrastructure needed to optimize PPA (performance, power, area) design and cycle times. These include electronic design automation (EDA) flows, silicon-proven libraries and IPs, simulation and verification design kits (also known as PDKs) and technology files.

For its advanced process technologies such as TSMC A16™, 2nm, 3nm, 4nm and 3DFabric®, the Company provides certified EDA tools and IP solutions that customers can use at various design stages to meet their product requirements. To help plan new product tape-outs incorporating library/IP from the Company's Open Innovation Platform® collaboration ecosystem, customers can use a portal to connect to solution providers, including 13 EDA partners, seven Cloud partners, 37 IP partners, 29 design center alliance (DCA) partners, and eight value chain aggregator (VCA) partners, as well as 23 partners with 3DIC expertise in the TSMC 3DFabric® collaboration alliance.

5.2.4 Design Enablement

Design enablement within TSMC's Open Innovation Platform® collaboration alliance is a critical component that focuses on providing customers with the necessary tools, methodologies and support to successfully create and verify their designs for manufacturing in TSMC's fabs. The Company's technology platforms provide a solid foundation to facilitate the design process for customers and acts as the bridge between a customer's innovative design idea and its successful realization in silicon and advanced package technologies. Customers can design using a combination of the Company's internally developed IPs and IPs and EDA tools as well as those available from Open Innovation Platform® collaboration alliance partners.

Tech Files and PDKs

EDA tool certification is an essential element to enable design for IP and to ensure that its features meet TSMC process technology requirements. Validation results and related information can be found on TSMC-Online. Corresponding technology files and PDKs for validation tools are available for customers to download and use with certified EDA tools. The Company provides a broad range of PDKs for digital logic, mixed-signal, RF, high-voltage driver, CMOS image sensor (CIS) and embedded flash technologies from 0.5μm to TSMC A16™ process technology. In addition, TSMC provides technology files for design rule (DRC) and layout versus schematic (LVS) checking, resistance-capacitance (RC) extraction, automatic place and route, and layout editing to ensure that process technology information is accurately represented in EDA tools. By 2025, the Company had provided customers with more than 58,000 technology files and around 4,000 PDKs.

Library and IP

Silicon intellectual property (IP) is the basic building block of IC designs. Various types of IP are available to support different customer design applications including foundation, analog/mixed-signal, embedded memory, interface and soft IP. TSMC and its alliance partners offer customers a rich portfolio of reusable IPs, which are essential building blocks for many circuit designs. To support 3DIC customer needs, the Company introduced 3DIC IP in 2019. By 2025, TSMC had expanded its library and silicon IP portfolio to contain around 93,000 titles from 0.5μm to TSMC A16™ process technology, a 12% increase over 2024.

Design Methodology and Flow

Design reference flows are developed using certified EDA tools to provide robust and comprehensive design methodology innovations that can help boost productivity. In 2025, the Company released TSMC A16™ digital and custom design reference flows through Open Innovation Platform® collaboration and announced their availability for customer adoption. In addition to process technology advancements, the Company released design reference flows for extending analog design migration from N2 to TSMC A16™ as well as N6RF+ to N4PRF for RF design migration, and continued to develop and offer 3DFabric® design solutions for both 3D chip stacking and 2.5D advanced packaging services. These included solutions supporting the IEEE P3537 standard to lower 3DIC design barriers, thus helping customers improve productivity in their system-level designs. These design reference flows feature solutions to optimize PPA and are integrated with AI and machine learning (ML) techniques that enable faster design creation and verification across various stages of the chip design flow.

5.2.5 Intellectual Property

For a long time, TSMC has been protecting R&D innovation and operation development by way of utilizing patents and trade secrets as dual tracks under the established comprehensive IP management system, encouraging Company's innovation culture, and strengthening Company's competitive strengths so as to fulfill the company's ESG vision. TSMC's General Counsel updates the Board of Directors on the status of the intellectual property management scheme.

TSMC's comprehensive patent management system includes: Patent management strategies, such as Global patent deployment, Exploratory invention mining, Patent portfolio expansion, and Patent exploitation and exercise; and Patent management rules, such as Tier-based IP evaluation, Patent competition rewards, Educational patent promotion, and Patent professional training. TSMC has established technological patent road maps by way of innovative patent strategy, strict management and risk-control measures; analyzed and monitored competitors by using intelligent patent maps; conducted core technology mining through invention workshops; expanded patent families on key technologies; filed and maintained patents by tier-based management, further enhanced patent protection through quality control on patent applications and continued to construct massive global patent portfolio with high quality; and, diversified exploitation of patent assets. In terms of patent filings, TSMC has accumulated more than 114,000 patent applications worldwide as of end of 2025, including more than 9,600 applications filed in 2025. TSMC ranked No. 2 among global U.S. patent applicants, and No. 1 among patent applicants in Taiwan. In terms of patent grants, TSMC has accumulated almost 79,000 patents worldwide as of end of 2025, including more than 7,700 global patents received. TSMC ranked No. 2 among U.S. Patentees, and No. 1 among patentees in Taiwan. In terms of patent quality, the allowance rate of TSMC's U.S. applications approached near 100%.

Turning to trade secret management and strategy, TSMC pioneered the "Trade Secret Registration System" in 2013 and was followed by the establishment of the "Trade Secret

Sustainable Intelligent Management Center" in 2024, which integrates eleven systems developed entirely in-house. In 2025, the "Trade Secret Innovation Talent Scouting Online Merge Offline Service" saw its services extended from front-end manufacturing to advanced packaging, strengthening the company's sustainable innovative culture and competitive advantage. TSMC identifies and rewards impactful and high-quality innovations through the annual Golden Trade Secret Award ceremony, having presented 3,858 Golden Trade Secret Award out of 656,387 registered trade secrets between 2013 and 2025, demonstrating immense innovative drive and potential. TSMC also established the "Green Trade Secret Registration" column in 2021, and to date recorded a total of 2,416 registrations, including 528 registrations made in 2025 alone, demonstrating TSMC employees' continuous emphasis placed on Green Trade Secrets. TSMC and the Allied Association for Science Park Industries jointly hosted the inaugural 2025 Trade Secret Intelligent Management Expo. Ten members of the Trade Secret Intelligent Management Alumni Association including TSMC, comprising of companies of varying industries and sizes, for the first time, presented real-world success stories through physical exhibition booths and public sharing forums, where they shared their experiences and insights on establishing trade secret registration systems and promoting intelligent management. The event attracted nearly 300 attendees from science park companies and other professionals interested in trade secret management.

TSMC received a AAA (the highest tier) certificate by Taiwan Intellectual Property Management System (TIPS) from Industrial Development Administration, Ministry of Economic Affairs in December 2021. The certification was successfully renewed in 2024, with validity from January 1, 2025, to December 31, 2027.

TSMC's IP team works closely with technical teams from R&D in early stage to mass production, and actively constructs IP portfolio for each key innovative technology, including the latest technology nodes, so as to ensure Company's technology leadership in semiconductor field; TSMC utilize patents and trade secrets as dual tracks to successfully protect Company's main business including process technologies, designs, manufacturing and sales, and have been strategically utilized for defense and cross-license negotiation, so as to secure freedom of business operation worldwide.

5.2.6 TSMC University Collaboration Programs

In recent years, TSMC has collaborated closely with several prestigious universities in Taiwan to carry out a variety of joint research projects. These collaborations encourage more university professors to conduct leading-edge semiconductor research in areas such as novel devices, process, materials manufacturing t echnologies, specialty technologies for electronic applications, and green manufacturing. At the same time, these projects provide hands-on training opportunities for interested students and prepare them to join the semiconductor industry after graduation.

Starting in 2013, TSMC established joint research centers at four top universities in Taiwan: National Yang Ming Chiao Tung University, National Taiwan University, National Cheng Kung University and National Tsing Hua University. In the past twelve years, more than 400 professors and 5,200 students with backgrounds in the disciplines of electronics, electrical engineering, physics, materials, chemistry, chemical engineering, and mechanical engineering have joined the research centers. In 2022, TSMC also actively supported the establishment of semiconductor or key technology research academies at National Taiwan University, National Cheng Kung University, National Tsing Hua University, National Yang Ming Chiao Tung University, National Sun Yet San University, and National Chung Hsing University, providing continuous funding for forward-looking research in Taiwan's semiconductor field and planning scholarship programs to encourage interested students.

In 2019, the Company jointly launched the TSMC-NTHU semiconductor program. By 2025, the list of school partners had grown to 19 universities with over 19,000 students enrolled. The institutions are: National Taiwan University, National Cheng Kung University, National Yang Ming Chiao Tung University, National Taipei University of Technology, National Taiwan University of Science and Technology, National Central University, National Sun Yet San University, National Chung Hsing University, National Chung Cheng University, Feng Chia University, Yuan Ze University, Chung Yuan Christian University, National Taiwan Normal University, National Yunlin University of Science and Technology, National Pingtung University of Science and Technology, National Kaohsiung University of Science and Technology, National University of Kaohsiung and National Kaohsiung Normal University.

In addition, TSMC has long conducted strategic research projects with over 30 top overseas institutions such as the Massachusetts Institute of Technology, Stanford University, Harvard University, the University of California, Berkeley, the National University of Singapore, Princeton University, Cornell University, the University of Chicago, Nanyang Technological University, the University of California, Los Angeles, the University of Tokyo, the University of California, San Diego and so on, all focusing on innovations in transistors, interconnects, materials, device simulation and circuit design.

TSMC University Shuttle Program

The TSMC university shuttle program was established to provide professors at outstanding research universities worldwide with access to the reliable silicon process technologies needed to develop innovative circuit design concepts. In 2025, TSMC expanded this industry-academia collaboration to include 7nm technology, connecting more research-driven professors, outstanding graduate students, and passionate TSMC executives. This initiative aims to foster the development of advanced silicon design, achieve innovation, cultivate a new generation of semiconductor talent, and promote close collaboration between industry and academia. The program provides TSMC's silicon process technology, supporting digital and analog/mixed-signal circuits, RF design, non-volatile memory, and ultra-low power design. In this way, TSMC and program participants achieve a win-win collaboration, allowing graduate students to realize exciting designs and demonstrate innovation in various end-product applications.

5.2.7 Future R&D Plans

To maintain its technology leadership, TSMC plans to continue investing heavily in R&D. While its A16 and A14 advanced CMOS logic nodes are progressing through the development pipeline, the Company's exploratory R&D work is focused on nodes beyond A14, as well as on areas such as 3D transistors, new memories, and low-R interconnect. This work aims to lay a strong foundation to foster the development of innovative technology platforms in the future. TSMC's 3DFabric® advanced packaging R&D is developing innovations in subsystem integration to further enhance advanced CMOS logic applications. The Company maintains an intense focus on new specialty technologies such as RF and 3D intelligent sensors for edge-AI and smart IoT applications. TSMC's research continues to develop novel materials and new processes, devices and memories that may be adopted in the longer-term future of ten years and beyond. The Company also continues to collaborate with external research bodies from academia and industry consortia, aiming for early awareness and adoption of future cost-effective technologies and manufacturing solutions. With a highly competent and dedicated R&D team and an unwavering commitment to innovation, TSMC is confident in its ability to drive future business growth and profitability for years to come by delivering advanced, competitive semiconductor technologies to its customers.

Summary of TSMC's Major Future R&D Projects

Project Name	Description
2nm logic technology platform and applications	3D CMOS technology platform for SoC
A16 logic technology platform	3D CMOS technology platform for SoC
A14 and beyond logic technology platform and applications	3D CMOS technology platform for SoC
3DIC	Cost-effective solutions with better form factor and performance for 3DIC integration
Next-generation lithography	Next-generation EUV lithography and related patterning technology
Long-term research	Specialty SoC technology (including new emerging memory NVM, MEMS, RF, analog) and transistors with 8 to 10 years horizon

The projects above account for roughly 89% of the total R&D budget for 2026. Total R&D budget is estimated to be around 7% of 2026 revenue.

5.3 Manufacturing Excellence

5.3.1 GIGAFAB® Facilities

In the semiconductor manufacturing industry, TSMC continues to play a pivotal role, with its core objective being to provide stable and reliable production capacity. Currently, TSMC operates four cutting-edge 12-inch Gigafabs: Fab 12, Fab 14, Fab 15, and Fab 18. As of 2025, the combined capacity of these four fabs has exceeded 13 million 12-inch equivalent wafers, offering process technologies covering the full generation and half-generation designs from 0.13 micrometers to 3 nanometers.

Looking ahead, TSMC continues to expand its advanced process footprint. While comprehensively deepening its 2-nanometer advanced production bases in Hsinchu and Kaohsiung, it is simultaneously expanding its advanced packaging capacity in Chiayi and Tainan, and actively

commencing the construction of its 1.4-nanometer fab in Taichung. These strategic deployments aim to flexibly respond to changes in market demand, providing the necessary wafer capacity support for the high-speed development of Artificial Intelligence (AI) technology and other applications.

Furthermore, to further strengthen its global service network, TSMC continues to expand its overseas production bases in Arizona, USA, and Kumamoto, Japan, and has established a new production site in Dresden, Germany. Through these global layouts, TSMC's global operations will become more mature and robust.

5.3.2 Quality and Yield Advancement

As advanced processes develop, integrated circuit linewidths continue to shrink, while diverse product portfolios deepen the challenges in process control. To pursue quality and manufacturing excellence, TSMC's process control system integrates multiple intelligent applications. Through Intelligent Detection, Smart Diagnosis, and Self-Learning, utilizing the latest information technology, it achieves the most stringent process control standards, thereby enabling TSMC to achieve remarkable results in yield improvement and quality control.

Concurrently, TSMC has long cultivated expertise in Artificial Intelligence (AI)-related fields, widely applying advanced technologies such as Machine Learning, Neural Networks, and Computer Vision to various production stages, including yield analysis, process control, equipment failure detection, virtual metrology, and wafer defect inspection, thereby achieving comprehensive optimization of production line scenarios. Building on this foundation, the company is also actively introducing Generative AI technology, which, by combining with semiconductor production expert knowledge, effectively accelerates advanced process variation detection and engineering analysis, thereby maximizing precise process control capabilities.

To continuously improve and expand, TSMC is extending its intelligent manufacturing system from the front-end fabs to the back-end fabs, establishing a complete process management chain from wafer to die at each production stage. Simultaneously, this intelligent manufacturing system has also encompassed all global fabs, to achieve comprehensive, consistent, and high-quality process management.

5.3.3 Production and Operations Efficiency

In response to the strong demand for high-end chips driven by applications such as High Performance Computing, Mobile, Automotive, and Internet of Things under the Artificial Intelligence trend, TSMC is committed to enhancing production capacity flexibility and equipment production efficiency while steadily expanding its fabs.

To support more flexible capacity deployment, TSMC continuously accelerates the deployment of its Automated Material Handling System (AMHS), significantly improving the efficiency and stability of production processes by extending automated handling services to connect fab areas, thereby substantially expanding production capacity. For the automated handling needs of advanced packaging production, TSMC has also successfully developed a new AMHS wafer carrier, which can flexibly support various back-end specific wafer carriers, ensuring smooth capacity expansion. In terms of strengthening operational resilience, TSMC is actively developing an "Automated Transfer Earthquake Prevention, Disaster Reduction, and Recovery System," which uses innovative technology to accelerate recovery efficiency after earthquakes, effectively addressing natural disaster challenges.

To maximize equipment production performance, TSMC integrates an AI architecture into its intelligent dispatching system. This not only optimizes the scheduling engine, giving it powerful parallel processing capabilities, but also successfully expands the scope of scheduling processing and significantly accelerates computing performance. Through these innovations, the company further solidifies and expands its leading edge over competitors in equipment production efficiency.

5.3.4 Digital Transformation

TSMC is deepening its digital transformation strategy, gradually evolving its automated factories into intelligent manufacturing bases. The core objective of this transformation is to empower employees, comprehensively enhancing their professional skills and overall value. Through the integration of virtual and physical technologies, the company is dedicated to improving employees' digital collaboration capabilities, enabling efficient collaboration among remote teams via smart wearables. Concurrently, TSMC is actively introducing robotic applications, employing innovative strategies to comprehensively boost personnel productivity.

At the same time, TSMC is also fully promoting the application of Low-Code platforms for operational process automation. This not only significantly lowers the technical barrier for system development but also allows years of accumulated semiconductor manufacturing experience to be quickly and effectively converted into standardized system processes. Concurrently, the company is deeply engaged in establishing information visualization and self-service analytics systems, assisting colleagues in unleashing their creativity to build customized reports and research tools, thereby achieving significant improvements in work efficiency and quality.

In summary, through a global intelligent manufacturing system and comprehensively empowered personnel digital capabilities, TSMC ensures a high degree of consistency in operational efficiency and manufacturing quality across all global fabs, ultimately achieving the grand goal of global integrated manufacturing.

5.3.5 Raw Materials and Supply Chain Management

In 2025, in collaboration with various fab operations, quality management, and related business units, TSMC continued to work hand in hand with suppliers to review and resolve issues related to capacity shortages, quality defects, and potential supply chain risks. Additionally, TSMC and its suppliers are committed to the development of advanced materials, process innovation, quality improvement, and supply chain energy conservation and carbon reduction, with the aim of promoting the development of a sustainable supply chain and achieving mutually beneficial outcomes.

Major Raw Materials Supply

Major Materials	Major Suppliers	Market Status	Procurement Strategy
Raw Wafers	A Company B Company C Company D Company E Company	Supply and demand equilibrium	• TSMC's suppliers of silicon wafers are required to pass stringent quality certification procedures. • TSMC procures wafers from multiple sources to ensure adequate supplies for volume manufacturing and to appropriately manage supply risk. • Raw wafer quality enhancement programs are in place to support TSMC's technology advancement. • TSMC regularly reviews the quality, delivery, cost, sustainability and service performance of its wafer suppliers. The results of these reviews are incorporated into subsequent purchasing decisions. • A periodic audit of each wafer supplier's quality assurance system ensures that TSMC can maintain the highest quality in its own products. • TSMC takes various approaches with suppliers to optimize cost and supply.
Chemicals	F Company G Company H Company I Company J Company	Supply and demand equilibrium	• Most suppliers have located their new operations closer to TSMC's major manufacturing facilities, thereby improving procurement logistics and reducing supply risk. • All supplied products are regularly reviewed to ensure that TSMC's specifications are met and product quality is satisfactory. • In order to effectively manage costs and supply chain, TSMC has collaborated with suppliers and adopted various strategies. • TSMC encourages and collaborates with chemical suppliers to implement innovative green manufacturing improvement programs.
Lithographic Materials	K Company L Company M Company N Company O Company	Supply and demand equilibrium	• TSMC works closely with suppliers to develop materials that meet all application and cost requirements. • TSMC and suppliers periodically conduct programs to improve their quality, delivery, sustainability and green policies, and jointly set improvement programs and monitor progress to ensure continuous improvement in TSMC's supply chain.
Gases	P Company Q Company R Company S Company T Company	Supply and demand equilibrium	• The majority of these suppliers have facilities in multiple geographic locations, which minimizes supply risk for TSMC. • TSMC conducts periodic audits to ensure that these suppliers meet TSMC's standards.
Slurry, Pad, Disk	U Company V Company W Company X Company Y Company	Supply and demand equilibrium	• TSMC works closely with suppliers to develop materials that meet all application and cost requirements. • TSMC and suppliers periodically conduct programs to improve their quality, delivery, sustainability and green policy, and jointly set improvement programs and monitor progress to ensure continuous improvement in TSMC's supply chain. • Most suppliers have relocated or plan to establish new manufacturing sites closer to TSMC's major manufacturing facilities, thereby improving procurement logistics and reducing supply risks.

Suppliers Accounting for at Least 10% of Annual Consolidated Net Procurement in 2025 and 2024

Unit: NT$ thousands

Supplier	2025			2024		
	Procurement Amount	As % of 2025 Total Net Procurement	Relation to TSMC	Procurement Amount	As % of 2024 Total Net Procurement	Relation to TSMC
Company A	27,209,602	26%	None	18,225,314	19%	None
Company B	20,552,324	19%	None	19,640,121	21%	None
Company C	10,271,830	10%	None	7,158,534	7%	None
Others	47,865,229	45%	-	50,596,085	53%	-
Total Net Procurement	105,898,985	100%	-	95,620,054	100%	-

- **Reason for Increase or Decrease:** The changes of procurement amount and percentage were mainly due to customer product demand change.

5.3.6 Quality and Reliability (Q&R)

TSMC strives to offer excellence in semiconductor manufacturing services to all its customers worldwide. The Company is dedicated to providing outstanding quality in every facet of its business and maintains a culture of continuous improvement to assure customer satisfaction. TSMC implements containment and preventive measures to protect customers from potential product defects.

In the technology development stage, the Q&R organization helps customers design in superior product reliability. In 2025, Q&R worked continuously with R&D in advanced logic, specialty and advanced packaging technologies throughout development and qualification stages to ensure meeting commitments to customers with respect to device characteristics, process yield and product reliability.

For advanced logic process technology, following the successful volume production of N3 and its performance-enhanced version N3P FinFET technology, Q&R also completed the process reliability qualification and product quality certification for N2 technology, the first nanosheet technology. For specialty technologies, Q&R achieved a critical milestone by qualifying the first high-voltage display driver integrated circuit (DDIC) process and product using N16 FinFET technology. Q&R also completed the qualification of N12 embedded RRAM technology for consumer grade and N16 embedded MRAM technology for automotive grade-1. In advanced packaging technology, TSMC has integrated front-end wafer fabrication with back-end chip packaging to provide advanced packaging solutions. The development focus has shifted from the original Si interposer technology to reconfigured interposers with multiple LSIs. In 2025, Q&R completed the certification of CoWoS® advanced packaging solution for 5.5x mask/reticle size interposers and will initiate volume production in 2026 to meet the higher performance targets of AI and HPC requirements. In the area of InFO_PoP technology, TSMC continues to lead the industry in the volume production of N3P-related chips, achieving higher efficiency and lower power consumption to support mobile applications.

To continuously reduce product defects, enhance process controls, facilitate early detection of abnormalities and prevent quality problems in general, Q&R collaborates with operational entities to improve real-time defense systems using advanced AI to continuously optimize quality tools through statistical methods. Q&R and the Company's fabs have also worked together on enhancements for automotive product quality improvement, including design rule extension and migration to Automotive Quality System 2.0. This covers process capability requirements to tighten in-line and wafer acceptance testing in fabs and the handling of maverick wafers. Q&R also provides dedicated resources for field/line return analysis and timely physical failure analysis (PFA) for process improvement to meet automotive customers' stringent defective parts per million (DPPM) requirements.

Q&R has actively advanced multiple digital transformation initiatives, covering areas such as laboratory tool and analysis automation, automatic defect detection and classification, intelligent statistical process control (SPC) and metrology. By leveraging advanced digital technologies and platform integration, Q&R has helped meet TSMC's digital transformation goals. Especially in light of the Company's ongoing expansion, digital transformation solutions have been employed to effectively address challenges related to employee needs. Looking ahead to 2026, Q&R will continue to promote automatic workflows and the application of AI to achieve quality and efficiency excellence, further strengthening TSMC's overall competitiveness.

Q&R's supply chain management strategy focuses on four core areas: quality excellence, responsible supply chain, green manufacturing and sustainable operations. While continuously assisting suppliers in making improvements based on professional expertise and best-known methods, Q&R's state-of-the-art chemical lab monitors the quality of raw materials and helps the R&D achieve breakthroughs in advanced materials.

In 2025, Q&R increased its emphasis on the "shared prosperity" strategy within its supply chain management approach. In addition to conducting quality audits for material suppliers, Q&R collaborated closely with colleagues from Intelligent Engineering Center, Nano-Materials Center, Material Supply Chain Management, Facility, and Material Technology Boards. Together, the team identified key suppliers for focused development and improvement and carried out onsite guidance visits. Unlike traditional audit supervision, TSMC's experts from various fields visited suppliers' production facilities to provide hands-on training and exercises on statistical process control (SPC) for management and frontline employees. The taskforce assisted in establishing real-time monitoring (RTM) systems for critical processes, offering resources and advice on production line automation design and investment strategies. Looking ahead to 2026, Q&R will continue to deepen this management strategy, progressively enhancing the quality management capabilities of the supply chain and driving its digital transformation. These efforts aim to ensure continuous improvement and strengthen the local competitiveness of the supply chain.

To enhance employee problem-solving skills and develop relevant quality systems and methodologies, TSMC implemented continuous improvement initiatives and organized company-wide competitions and training programs. To strengthen TSMC's quality culture, Q&R began offering quality culture courses for new employees in 2022. These courses help new employees establish correct quality values and accelerate the integration and adaptation to their roles. In addition to internal cross-organizational learning and sharing, TSMC participates in the Taiwan Continuous Improvement Awards (TCIA) to promote the development of other local industries by sharing its experiences. In 2025, TSMC's outstanding performance was recognized with five gold, three silver and four "best improvement and innovation" awards. Meanwhile, Q&R encouraged local material suppliers to participate in the TCIA for capability and quality culture enhancement, and they won a total of three gold, two silver, five bronze medals and two "best improvement and innovation" awards.

Thanks to qualification in technology development, real-time defense systems and innovative applications in semiconductor manufacturing services, as well as its continuous quality improvement culture, TSMC had no product recalls initiated by customers due to safety concerns in 2025. Meanwhile, a third-party audit verified the effectiveness of the Company's quality management systems in compliance with IATF 16949: 2016 and IECQ QC 080000: 2017 requirements. In 2025, TSMC's backend fabs also continually passed the certification of American National Standards Institute ANSI/ESD (electrostatic discharge) S20.20 standard. Regular customer feedback indicates that products shipped from TSMC have consistently met or exceeded all field quality and reliability requirements. In these ways, TSMC helps customers improve time-to-market delivery and competitiveness with excellent, reliable products for the major growth markets that the Company serves: HPC, smartphones, IoT, automotive, and digital consumer electronics.

5.4 Customer Trust

5.4.1 Customers

TSMC has customers with wide-ranging product portfolios who are top-tier in each sector within the semiconductor industry from all over world, including fabless semiconductor companies, system companies, and integrated device manufacturers.

Customer Service

TSMC is committed to providing customers with the highest quality service. The Company believes that excellent customer service is key to maintaining and improving customer satisfaction, solidifying existing customers, and attracting new customers. To this end, TSMC has established a dedicated customer service team to act as the primary contact window, facilitating seamless communication and coordination with customers in areas such as product design, mask making, wafer manufacturing, and 3DFabric® technology services, ensuring worldclass service every step of the way. TSMC is committed to continuously improving customer satisfaction, earning customer trust, maintaining sales and profitability, and solidifying its role as one of the most reliable partners.

To improve customer interaction on a real-time basis, TSMC-Online offers a suite of web-based applications to provide more proactive customer service and support in design, engineering and logistics. Customers thus have 24-7 access to critical information. TSMC-Online facilitates design collaboration by maintaining data availability and accessibility and providing customers with accurate up-to-date information at each stage of the design process. Engineering collaboration focuses on wafer, and 3DFabric® technology service includes processes, yield and wafer acceptance test analysis, as well as data quality and reliability. Logistics collaboration includes information on wafer fabrication, advanced packaging, testing, and transportation. In addition, customers can generate customized reports through TSMC-Online to meet their system automation needs.

Customer Satisfaction

To ensure customer satisfaction, TSMC must fully comprehend its customers' needs. To this end, the Company works with third-party consulting firms to conduct annual customer satisfaction surveys (ACSS) with the majority of existing customers, either via online surveys or in direct interviews. In addition to the survey, TSMC also conducts quarterly business/technical reviews (QBR/QTR) with customers to collect their feedback on a regular basis. Customer feedback is routinely reviewed, analyzed and used to develop appropriate improvement plans, all in all becoming an integral part of the customer satisfaction process. Through surveys and feedback reviews, TSMC is able to closely interact with customers, provide better services, and enhance the quality of customer collaboration.

Customer Information Protection

TSMC complies with applicable regulations and international standards to protect customer information and has received ISO 27001 international information security certification. In addition, relevant proprietary information protection policies and standard work processes are also established to ensure only authorized personnel can access the engineering and production data of any specific customer.

Customers Accounting for at Least 10% of Annual Consolidated Net Revenue in 2025 and 2024

Unit: NT$ thousands

Customer	2025			2024		
	Net Revenue	As % of 2025 Total Net Revenue	Relation to TSMC	Net Revenue	As % of 2024 Total Net Revenue	Relation to TSMC
Customer A	726,974,278	19%	None	352,271,213	12%	None
Customer B	645,178,671	17%	None	624,345,477	22%	None
Others	2,436,901,323	64%	-	1,917,691,009	66%	-
Total Net Revenue	3,809,054,272	100%	-	2,894,307,699	100%	-

- **Reason for Increase or Decrease:** The changes of sales amount and percentage were mainly due to customer product demand change.

5.4.2 Open Innovation Platform®

At TSMC innovation is a core value and is fostered through the Open Innovation Platform, a key component of the TSMC Grand Alliance. The Open Innovation Platform® collaboration alliance initiative facilitates active collaboration with external partners through an "outside in" approach to complement traditional "inside out" methods.

The Open Innovation Platform® collaboration alliance is a comprehensive design technology infrastructure that encompasses all critical IC implementation areas to lower design barriers, improve cycle times and raise first-time silicon success rates. Through the use of TSMC process technologies and partnered solutions, Open Innovation Platform® collaboration alliance promotes the rapid adoption of cutting-edge innovation within the semiconductor industry.

Crucial to Open Innovation Platform® collaboration alliance are ecosystem interfaces and collaborative components initiated and supported by TSMC to empower innovation throughout the supply chain. Also key is TSMC's active accuracy assurance (AAA) initiative, which provides the precision and quality required by the ecosystem interfaces and collaborative components.

TSMC's Open Innovation® collaboration brings together the creative thinking of customers and partners under the common goal of shortening each of the following: design time, time to volume production, time to market and, ultimately, time to revenue. The model features:

- The EDA alliance, launched in 2011, stands as the foundry segment's earliest and most comprehensive electronic design automation certification program. It encompasses all stages of advanced IC and package development, provides design reference flows for innovative methodologies, and ensures timely design tool readiness for new process technologies.
- Established with the initiation of Open Innovation Platform® collaboration alliance in 2008, the IP alliance delivers the foundry segment's most comprehensive and robust portfolio of silicon-proven intellectual properties and libraries. IP quality assessment requirements are conducted through the TSMC 9000 program and the library quality and management program.
- Launched in 2018, the cloud alliance accelerates time-to-market for IC and system design by facilitating cloud-based semiconductor design. This enhances scalability, agility and flexibility, meeting diverse customer requirements. EDA on cloud certification is also available for market-leading cloud service provider (CSP) infrastructures.
- Also established within Open Innovation Platform® collaboration alliance from the beginning, the design center and value chain alliances provide comprehensive design services. They support customer demand for resources and capabilities across various semiconductor design stages and the entire value chain, adapting to diverse project scopes and requirements.
- The TSMC 3DFabric® alliance, launched in 2022, is the latest addition. It encompasses partners across EDA, IP, test, DCA/VCA, memory, substrate and OSAT. Its mission is to drive innovation and readiness in the 3DIC ecosystem, enabling customers' system-level designs by integrating multiple chips/chiplets through 3D stacking and advanced packaging.
- Open Innovation Platform® collaboration alliance participants include 13 EDA partners, seven cloud partners, 37 IP partners, 29 design center alliance (DCA) partners, eight value chain aggregator (VCA) partners and 23 partners in the TSMC 3DFabric® alliance.
- A partner management portal facilitates communication with ecosystem partners for efficient business productivity – designed with a highly intuitive interface and accessible via direct link from TSMC-Online.

TSMC and its partners work together proactively and engage earlier and deeper than ever before to address the mounting design challenges of advanced technology nodes. Through this early and intensive collaboration, Open Innovation Platform® collaboration alliance delivers the needed design infrastructure with timely readiness of EDA tools, early availability of critical IPs, and quality design services when customers need them. Taking full advantage of the process technologies once they reach production-ready maturity is key to customer success. This enables TSMC process technologies, Open Innovation Platform® collaboration alliance design solutions, and customer product designs to synergize for design technology co-optimization (DTCO). The availability of these design ecosystem solutions helps customers successfully pursue opportunities in all major markets: HPC, smartphones, IoT, automotive and digital consumer electronics.

The 2025 annual Open Innovation Platform® Ecosystem Forum, conducted in North America and elsewhere around the world, demonstrated how the Company and its ecosystem partners jointly develop design solutions on top of TSMC's advanced technologies through Open Innovation Platform® collaboration alliance. At the forum, TSMC made key presentations on its comprehensive 2nm technology family and TSMC A16™ process technology that continue the full-node PPA scaling trend, together with offering high-density and

high-performance libraries and design solutions to support smartphone and HPC design applications. The Company also made presentations on the readiness of analog cells that can help boost IP yields and analog design productivity, with design solutions to enable EDA and design flow automation to support analog design migration. At the forum, the Company highlighted expanded collaboration with ecosystem partners to drive AI applications that improve design quality and productivity.

In response to the rising demand for more complex system level designs, TSMC collaborates with TSMC 3DFabric® alliance partners, who have 3DIC expertise in EDA, IP, DCA/VCA, test, memory, substrate, and outsourced semiconductor assembly testing (OSAT) to provide 3D chip stacking and 2.5D advanced packaging design solutions. These, together with EDA tools compliant to the IEEE P3537 open standard, facilitate integration of multiple chips/chiplets in system-level designs using TSMC 3DFabric® advanced packaging services, which include TSMC-SoIC®, CoWoS®, TSMC-SoW™, and TSMC COUPE™, and achieve system and process co-optimization.

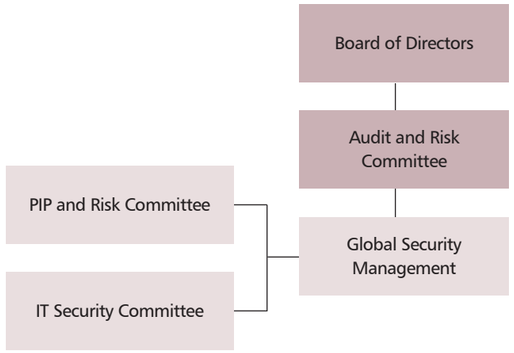
5.5 Information Security Management

5.5.1 Information Security Policy and Organization

TSMC is committed to information security and confidentiality protection for its customers, shareholders and partners. To this end, the Company has formulated, implemented and regularly updated rigorous information security policies, procedures and measures as reflected in TSMC's information security declaration.

In 2022, following the regulations of the Financial Supervisory Commission of Taiwan, TSMC created the role of Chief Information Security Officer (CISO). Starting from 2025, TSMC appointed Cliff Hou, Senior Vice President and Deputy Co-COO as CISO, responsible for overall planning and coordination of Company resources and for communicating on information security policies and directions. TSMC has established a dedicated global security management (GSM) organization, to be responsible for the implementation, planning, monitoring and management of information security. TSMC's PIP and risk committee and the IT security committee cooperate with the Company's IT and related organizations to strengthen corporate information protection and management mechanisms. Both committees are chaired by the CISO and comprise VP-level executives who meet regularly to review and deliberate on important information security policies as well as project implementation. Every six months, GSM executives report risk management measures to the Audit and Risk Committee, including global information security trends, corporate information security policies, plans, and implementation results. In turn, the chair of the Audit and Risk Committee reports to the Board of Directors on the effectiveness of information security supervision and risk control measures throughout the Company.

Global Security Management Organization Structure



5.5.2 Information Security Management Strategy and Resources

To achieve TSMC's information security goals and maintain competitiveness, the Global Security Management organization actively strengthens information security, confidential information protection mechanisms and physical security management. GSM sets clear policy, procedures and guidelines, continuously enhances the Company's management systems, and implements comprehensive risk controls. In addition, GSM regularly performs information security risk assessments and sets priorities based on the impact and probability of a risk, as well as the cost of reducing such risk. GSM uses the plan-do-check-act (PDCA) methodology to continuously enhance multi-layer information security defenses and establish key performance indicators (KPIs) for information security. In 2025, TSMC invested in excess of NT$1 billion to strengthen information security, involving more than a thousand employees for information security-related activities, with more than 1,800 external security personnel engaged in the physical aspects of information security services.

5.5.3 Information Security Incident Handling and Notification

TSMC has established enterprise risk management mechanisms and procedures to handle information security incidents. The mechanisms and procedures define relevant processes and measures for incident notification, designation of personnel responsible for handling material information security incidents, and assessment of losses suffered as well as additional measures needed, evaluation of potential impacts of information security risks to the Company's financial and operations, and proposed countermeasures to mitigate these risks. In 2025 and as of the date of this Annual Report, TSMC has not suffered any financial losses, nor experienced any operational impact, due to material information security incidents.

5.6 Human Capital

Human capital is TSMC's most treasured asset. The Company strives to provide employees with meaningful work, continuous learning, a healthy and inclusive workplace, and high-quality compensation and benefits. TSMC goes beyond this by actively encouraging employees to nurture and enjoy a healthy family life, develop personal interests, expand social participation, and, in general, live a happy life.

5.6.1 Human Rights Policy and Specific Actions

TSMC strongly believes that respecting human rights and promoting a safe, respectful work environment are vitally important. The Company is committed to supporting international human rights standards while complying with local laws in all operating locations, treating and respecting all personnel equally. The TSMC human rights policy applies to the management team and all employees (those employed by TSMC and receiving wages or compensation), affiliated enterprises, suppliers, contractors, and partners including customers and communities, as well as all other stakeholders committed to eliminating human rights violations.

Management Principles

- Human Rights Governance Structure

TSMC has established a human rights governance structure with the Board of Directors at the highest level. The ESG committee has established a cross-department human rights taskforce, encompassing customer service, corporate sustainability, environmental safety and health, human resources, information technology, corporate information security, materials management, legal, operations, quality and reliability, research and development and other functional organizations to systematically and effectively promote human rights management activities. In addition to regularly reporting progress to the ESG steering committee, the chairperson of the ESG committee reports to the Nominating, Corporate Governance and Sustainability Committee under the Board of Directors on human rights management actions and implementation results.

- Due Diligence

TSMC follows the recommendations of the OECD guidance for responsible business conduct to carry out the Company's due diligence process. TSMC conducts the due diligence process by embedding responsible business practices into its policies and management systems, regularly identifying and assessing risks, implementing prevention and mitigation measures, and tracking mechanisms.

- Training and Advocacy

TSMC has developed human rights protection training to establish awareness and develop a culture of respecting human rights. Through such training, the Company informs employees about human rights concepts and their importance, accessible grievance channels available to all, and TSMC's measures for the handling, prevention, and remediation of human rights violations.

- Grievance Channels

TSMC has established robust grievance and communication channels and is committed to protecting complainants. Potential human rights violations can be reported anonymously or through a variety of communication mechanisms to express concerns or suspected violations to TSMC, and the Company is committed to initiating appropriate follow-up actions.

- Remediation

Once a human rights violation is identified, the Company will initiate a remediation mechanism based on the type of incident and, if necessary, cooperate with relevant stakeholders to prevent recurrence.

- Communication and Disclosure

TSMC identifies affected individuals on a case-by-case basis based on salient human rights issues to build a solid, trusting relationship, and listens to the voices of stakeholders through diverse and open two-way communication channels. The Company regularly discloses human rights management goals, actions, performance, and progress in its sustainability and human rights reports on the Company's ESG website.

In 2025, the Company used the Responsible Business Alliance's self-assessment questionnaire (SAQ) to identify the greatest risks regarding labor, health and safety, environment, and ethical matters and to formulate substantive actions and managerial response. The SAQ scores of each of TSMC's operating fabs in Taiwan were in the low-risk range (defined as 80 points or above).

TSMC actively fosters employees' fundamental understanding of business and human rights and strengthens their understanding of the Human Rights Policy. In 2025, TSMC offered an online course: "TSMC Human Rights Policy – Build a Workplace Free of Sexual Harassment" with 80,938 participants completing the training, respectively. The Company expects employees to integrate respect for human rights into their daily decisions and actions, thereby fulfilling its human rights commitments.

TSMC abides by laws and regulations and respects the freedom of collective consultation, assembly and association of all employees. The Company will not interfere or intervene with these activities. TSMC holds Silicon Garden (labor-management) meetings on a regular basis, listens to employees' opinions and makes timely and appropriate responses through a diversified and comprehensive internal communication framework, in order to strengthen communication between the management team and employees and ensure harmonious employee relations.

5.6.2 Inclusive Workplace

TSMC is dedicated to accelerating innovation to address some of the world's most complex technological challenges. This requires a culture that encourages contributions from all employees, at every level, in any role, regardless of their background or identity. Building an inclusive workplace reflects TSMC's core values and business philosophy. Through actively promoting an open-style management approach, the Company encourages diverse talents to join the semiconductor industry.

In accordance with TSMC's global inclusive workplace statement and its people vision, the Company has committed to three key endeavors: delivering an inclusive experience throughout the employee lifecycle, empowering diverse talents through employee resource groups (ERGs), and fostering connections with external resources and partners. At every stage of an employee's lifecycle, TSMC examines the procedures and policies to ensure recruitment channels and development opportunities are in place to promote diversity.

In 2025, TSMC continued to host the GIW (Global Inclusive Workplace) Month series of initiatives to foster a strong sense of belonging and promote allyship among employees. In addition, the Company has expanded the Inclusion Champion program to a global scale, encouraging colleagues worldwide to take meaningful and actionable steps toward inclusion. As part of the ongoing commitment to support diversity – in addition to Women@tsmc, Global Family@tsmc, Accessibility@tsmc, and the U.S.-based Veterans@tsmc – TSMC launched Pride@tsmc at its headquarters. These ERGs champion diversity topics across gender, sexual orientation, race and nationality, disability, and the U.S. protected veterans. ERGs are open to all employees, regardless of whether they possess the relevant identity, allowing all employees to participate and show their support, aiming to enhance their sense of belonging. As for connecting with external resources, the Company benchmarks with international standards and establishes partnerships with professional organizations to ensure alignment with global best practices. TSMC's strategic partnerships include global organizations such as the Global Semiconductor Alliance (GSA) and Disability: IN. The Company also collaborates with Out & Equal to advance LGBTQ+ inclusion and has deepened its involvement with GSA Talent Initiative (GTI) to promote female leadership in STEM areas and encourage broader industry participation. Additionally, TSMC has enhanced stakeholder communication and transparency through the redesign of websites.

TSMC has also developed a learning structure and core training courses by job level for all employees. The aim is to help employees understand the essence of inclusion, encourage them be mindful of unconscious biases, cultivate their ability to identify and respond appropriately to biases while enhancing their awareness of this topic. In addition, the Intercultural Intelligence Program was launched to empower employees to work effectively with peers from diverse backgrounds.

5.6.3 Workforce Structure

At the end of 2025, TSMC had 90,557 employees worldwide, including 9,582 managers, 44,690 professionals, 11,368 assistants and 24,917 technicians. The following two tables summarize the makeup of TSMC's workforce and the female portion of management as of the end of February 2026:

Workforce Structure

		12/31/2024	12/31/2025	02/28/2026
Job	Managers	8,737	9,582	9,744
	Professionals	40,477	44,690	45,064
	Assistant Engineer/Clerical	10,207	11,368	11,451
	Technicians	24,404	24,917	25,094
Total		83,825	90,557	91,353
Gender	Male	66.3%	67.0%	67.0%
	Female	33.7%	33.0%	33.0%
Education	Ph.D.	3.7%	3.6%	3.6%
	Master's	48.5%	49.8%	50.0%
	Bachelor's	29.9%	29.7%	29.7%
	Other Higher Education	7.5%	7.0%	6.9%
	High School	10.5%	9.9%	9.8%
Average Age		36.2	36.3	36.4
Average Years of Service		8.7	8.9	8.9

Female Ratio in Management

	12/31/2024	12/31/2025	02/28/2026
Female Ratio in Junior Management	15.0%	15.6%	15.6%
Female Ratio in Senior Management	14.0%	14.1%	14.2%
Female Ratio in Top Management	11.4%	6.3%	5.7%

Note: Junior management positions include first-line managers; top management positions include vice presidents and higher as well as the CEO.

5.6.4 Recruitment

TSMC believes growth and success depend on its employees sharing a common vision and values. As an equal opportunity employer, the Company is committed to searching for and hiring top professionals in all positions through an open and fair recruitment process. In addition to prioritizing integrity and ability as the primary conditions for employment, TSMC also considers suitability for the position, evaluating all candidates equally regardless of nationality, race, class, language, belief, religion, political party, place of ancestry, place of birth, gender, sexual orientation, age, marital status, appearance, facial features, and physical and mental disabilities.

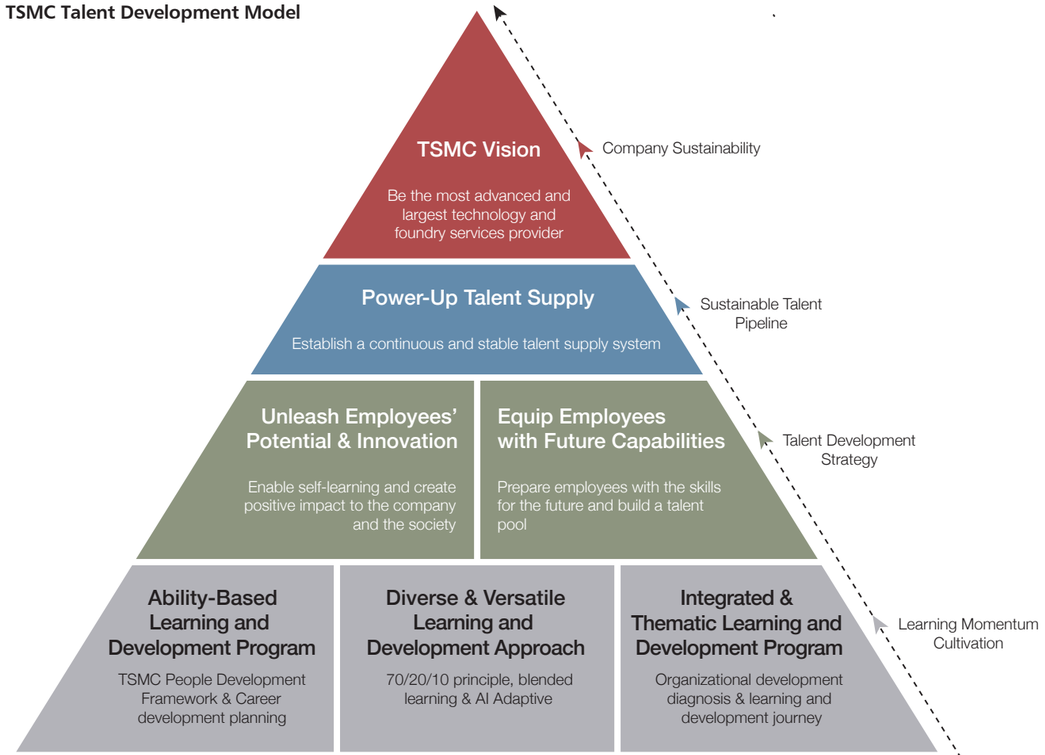
TSMC adheres to its core values and continues to move towards its lofty vision. To ensure the talent it needs for continuous growth, the Company keeps expanding its recruitment channels to attract top professionals in all positions. In 2025, TSMC employed over 9,200 people worldwide.

5.6.5 People Development

TSMC firmly believes that talent is the basis of the Company's growth and is committed to realizing its People Vision by inspiring and enabling employees to perform their best in the workplace. This, in turn, helps establish a continuous and stable talent supply system, ensuring the Company's long-term competitiveness and sustainable development. To achieve this vision, TSMC has developed its "TSMC Talent Development Model" as the cornerstone, featuring two major strategies: (1) unleashing employees' potential and innovation, i.e. enabling self-learning and creating positive impact to the Company and the society, and (2) equipping employees with future capabilities, i.e. preparing employees with the skills for future work and building a talent pool.

Following these talent development strategies, TSMC has initiated ability-based learning and development programs. In addition to focusing on the core attributes of character, perseverance, resilience, initiative, innovation, decisiveness and judgment, broadness of mind and breadth/depth of knowledge, the Company also integrates career planning to develop colleagues' leadership, professional and general skills according to different positions and professions, and the Company's organizational needs. At the same time, TSMC offers diverse and versatile learning and development approaches, utilizing the 70/20/10 principle of experiential learning (70%), feedback and guidance (20%), and education and training (10%), supplemented by blended learning and future AI adaptive learning. Furthermore, in response to the increasingly complex organizational ecosystem and diverse needs, TSMC proactively plans for talent, starting with organizational development diagnostics to customize learning and development journeys for different roles, levels, and organizations, integrating and systematically cultivating the capabilities required by employees, thereby supporting employees and TSMC in achieving continuous growth and breakthroughs.

TSMC Talent Development Model



In 2025, TSMC offered 10,079 in-person courses, including both face-to-face and live online, and 40,410 online learning resources, including internal and external learning platforms, providing over 8.18 million hours of training with an excess of 3.57 million participants. The average annual training time per employee is 90.4 hours. TSMC training expenses reached NT$1.38 billion in 2025 and the average training cost reached NT$15,200 per employee, a 23.1% increase over the previous year (Note).

Note: In order to align the definition of training expenses with international market research information (as in Training magazine) to include total training spending, outside products and services, and training staff payroll, starting in 2022 the Company began including training staff payroll in annual training expenses.

5.6.6 Competitive Overall Compensation

In order to develop the most effective compensation strategies, TSMC benchmarks companies annually and collects market information on compensation data of the whole industry for competitive analysis. TSMC's compensation program includes a monthly salary, performance bonuses based on quarterly business results, and profit sharing based on annual results.

The purpose of the business performance bonus and profit sharing programs is to reward employee contributions appropriately, to encourage employees to work consistently toward ensuring TSMC's success, and to align employee interests with those of TSMC's shareholders so as to achieve win-wins for the Company, shareholders and employees alike. The Company determines the bonus and profit sharing amounts based on operating results and domestic industry practice. The amount and distribution of employee bonuses are recommended by the Compensation and People Development Committee to the Board of Directors for approval. Individual rewards are based on each employee's job responsibility, contributions and performance. A similar approach is used in TSMC's compensation programs at its subsidiaries. In addition to providing employees with a locally competitive base salary, annual bonuses are granted as a part of total compensation, in line with local regulations, market practices and the overall operating performance of the subsidiary.

In addition to the competitive compensation described above, the Company established a global employee stock purchase plan in 2022, which is available to all regular employees of TSMC and its wholly owned subsidiaries. In 2024, the Company extended participation to employees of majority-owned subsidiaries as well. Through this plan, employees are encouraged to participate in the Company's long-term success.

To strengthen the link between TSMC executives and shareholders' interests, the Company established corporate officer shareholding guidelines in 2020. The required holding value of TSMC shares by the chairman, CEO, and corporate officers is proportional to their annual base salary: 18 times for the chairman and CEO, nine times for officers in Taiwan and three times for officers overseas. Officers must reach the required value within three years of appointment and maintain it for the entire period of employment. Furthermore, to attract and retain corporate executives and other critical talent and to link their compensation with shareholder interests and environmental, social, governance (ESG) achievements, TSMC established employee restricted stock awards for each year from 2021 to 2024.

Effective in 2025, TSMC will implement an annual Long-Term Incentive (LTI) bonus plan. This plan expands the scope of performance indicators beyond the existing linkage to shareholder interests and ESG achievements, to also include company financial indicators. Through these diverse and clear quantitative metrics, the plan aims to strengthen management's long-term and continuous creation of company revenue and shareholder value, concurrently enhancing ESG performance.

5.6.7 Employee Benefits Exceed Legal Requirements

TSMC generally offers employee benefits superior to those required by applicable statutes. In addition to twelve national holidays per year, additional memorial days are also designated as holidays. To alleviate traffic congestion during commuting hours, support family care needs, and create an inclusive workplace, the Company implemented a staggered commuting policy in 2023, which is continuously optimized. To encourage employee participation in the Company's vision of "making society better," TSMC provides one day of volunteer leave per year starting in 2023. The Company provides employees with statuary labor insurance and national health insurance as well as comprehensive paid group insurance plans. Coverage includes life insurance and insurance for accidents, hospitalization, cancer, critical illness, maternity and international business travel. There are also various, unique self-paid group insurance plans available for employee family members. The group insurance coverage is extended to employees on approved unpaid leave. To support new hires, TSMC offers one day of annual leave for every two months of service in the first year. Employees who need to take long leaves of absence for military service or health reasons can also apply for unpaid leave, and then apply for reinstatement after the expiration of the period. TSMC provides pensions, financial assistance for emergencies, subsidies for marriage, childbirth and funerals, as well as discounts in designated shops. In response to the continuous growth and diversification of its workforce, and to enhance support for employees' lives and family care, the Company launched its global flexible benefit plan (tFlex) in 2024, building on its existing benefits system. This plan is divided into four main categories: medical and insurance, family care, wellness, and development and volunteering. The plan offers each full-time employee worldwide flexible benefit points equivalent to around US$250 per year. For employees in Taiwan, it's equivalent to NT$8,000. Employees can freely choose and redeem benefits that align with their lifestyle.

In accordance with local laws and regulations, TSMC provides lactation rooms. To help employees balance their personal and work lives, TSMC not only offers parental leave but also provides a comprehensive leave management system. In 2023, the Company enhanced its TSMC Childcare benefit program 2.0, extending maternity leave for a second birth from 12 to 16 weeks and for a third birth from 16 to 20 weeks. TSMC also offers a maximum maternity subsidy of NT$20,000 (NT$10,000 from the employee welfare committee plus up to NT$10,000 from maternity insurance).

To further cultivate a family-friendly workplace, TSMC introduced childcare benefit program 3.0 in 2024, with official implementation at its Taiwan fabs starting in 2025. This comprehensive program delivers corresponding resources for every stage – from pre-pregnancy, pregnancy, and childbirth to early childhood (below age 1, ages 2-6, and under age 12). It also offers valuable fertility education sessions and parenting consultation services, aiming to provide holistic support to employees at every family stage. Beyond these programs, TSMC has set up four onsite kindergartens for employees in Taiwan. In addition, a holiday STEAM (science, technology, engineering, art and math) campus has been organized for employees' children.

All TSMC fabs are equipped with a 24-hour wellness center, where occupational health professionals (physicians, nursing practitioners, psychologists) and appointed onsite physicians provide quality services beyond those required legally. The wellness centers work with hospitals and employee assistance providers to offer comprehensive support for the emotional and physical well-being of employees. In addition to annual checkups for all employees, TSMC provides employees with five advanced checkup items upon completion of every five years of service.

- The Company encourages employees to exercise regularly by subsidizing approximately 70 clubs or exercise facilities and holding regular sports events to help employees find peers with similar sports interests.
- To help employees balance their work and life, TSMC provides convenient onsite services and amenities such as in-fab cafeterias, convenience stores, and other services.
- TSMC provides comprehensive health management services, including in-fab clinic services, post health-exam follow-up activities, and employee assistance programs.
- TSMC also offers diverse employee welfare programs, leisure and art events, hobbyist clubs, vibrant sports centers and onsite preschool services to meet employees' needs for childcare, festival bonuses and emergency subsidies.

Vacation and insurance policies at TSMC's overseas offices are designed to comply with local regulations. In China, North America and Europe, TSMC provides more vacation days to employees than legally required. In overseas offices, TSMC offers a more comprehensive life and medical insurance than required by local regulations and customs.

5.6.8 Diverse Employee Recognition

TSMC sponsors various internal award programs to recognize employees for outstanding achievement and significant contribution, both individual and at a team level. The aim of these award programs is to encourage continued employee development, which also enhances the Company's competitiveness. Examples include:

- TSMC Academy award for outstanding scientists and experts for individual technical contributions
- TSMC Excellent Employee award for technicians' for outstanding performance
- Various recognitions for excellence and continuous improvement
- Service award to show appreciation for employees' long-term commitment and dedication
- Excellent Trainer Award for the outstanding contribution by internal trainers of training courses

In addition to the recognitions above, there are function-wide awards dedicated to innovation, such as the Idea Forum, the Total Quality Excellence Conference and the ESG Award, which recognize employee initiative and continuous implementation of innovative practices. Furthermore, TSMC encourages employees to participate in external awards and competitions. In 2025, distinguished TSMC employees continued to be recognized through a host of awards, such as the Model Labor award, the Taiwan Continuous Improvement awards, the National Manager Excellence award, the National Industrial Innovation awards, and the Executive Yuan award for outstanding science and technology contribution.

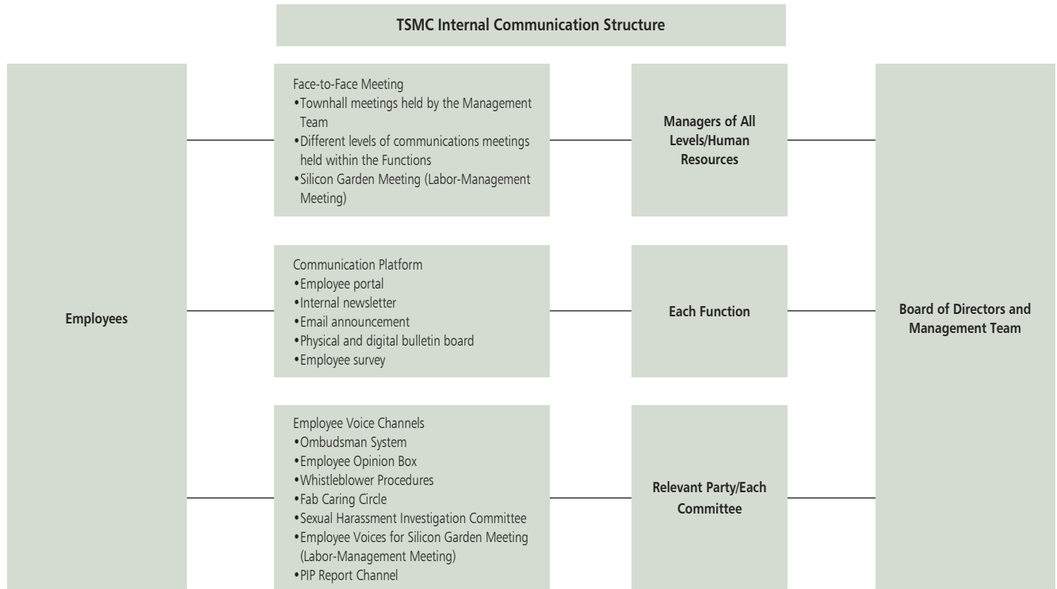
5.6.9 Employee Engagement

TSMC is committed to creating a fun and dynamic workplace. Through a diverse series of initiatives, the Company continues to enhance employee engagement.

TSMC provides a wide variety of communication channels, including:

- Townhall meetings held by management teams and communication meetings held within various functions;
- Quarterly Silicon Garden (Labor-Management Meeting) to provide business updates and discuss issues of concern;
- A biennial global survey conducted to promote understanding of the Company's core values from the employees' perspective;
- A biennial global survey to promote understanding of employee engagement and work experience;
- Periodic employee pulse surveys and service satisfaction surveys given to selected employees with follow-up actions based on survey findings;
- myTSMC employee portal - an internal website featuring talks by the founder and former Chairman as well as the Chairman and the CEO, corporate messages, announcements of recent activity and other topics of interest to employees;
- eSilicon Garden reports on significant Company activities and stories of outstanding teams or individuals to deepen employees' connection with the Company's core values;
- Three channels for reporting complaints regarding managerial, financial, auditing, ethics and business conduct issues:
  - The whistleblower reporting system, the complaints are received directly by the Chairman of the Audit and Risk Committee (an independent director);
  - The irregular business conduct reporting system, administered by the Ethics committee;
  - The ombudsman system, administered by a senior manager, appointed by the CEO;
- The employee opinion box, which provides an opportunity to submit suggestions or opinions regarding work and the work environment;
- The fab caring circle in each fab, which addresses issues related to employees' work and personal life – dedicated mainly to the Company's direct laborers;
- The sexual harassment investigation committee – consisting of three directors appointed by the CEO, one from human resources, one from legal affairs, and the third from another organization – acting as a channel to ensure the work environment free from the threat of sexual harassment. Taiwan also establishes an investigation team, including external experts, in accordance with governmental regulations to conduct case investigations.

Employee Communication Channels



During 2025 and as of the date of this Annual Report, TSMC has not incurred any labor-dispute related losses. However, the Company was fined three times for the extension of working hours combined with the regular working hours exceeding permitted limit (Labor Standards Act Article 32 Paragraph 2): NT$350,000 on 02/14/2025, NT$400,000 on 04/17/2025, NT$450,000 on 05/08/2025, and NT$450,000 on 09/04/2025.

The Company has reviewed its working hour management process and established indices to remind employees to apply for overtime payment on time and for mangers to respond to such applications efficiently and in a timely fashion, and to be more diligent about employee working hours as well as to strengthen communication about these matters and relevant policies.

5.6.10 Retention

IIn 2025, TSMC conducted a global engagement survey of 76,279 full-time employees including subsidiaries, which achieved a high response rate of 88%. Compared to the 2023 survey results, TSMC's employee experience showed significant improvement across all four dimensions: Vision Alignment, Work Effectiveness, Overall Compensation, and Team Leadership. Furthermore, TSMC employees' confidence in the leadership team, the company's overall competitiveness in the market, their feeling of empowerment, growth opportunities, and their satisfaction with compensation have exceeded the benchmark of global top-performing companies. This further solidified employee trust and satisfaction. It's worth mentioning that in the area of "Sustainable Engagement," we have achieved a historic milestone, having outperformed global top-performing companies.

Looking ahead, TSMC will continue to focus on improving employee experience and collaborating with all colleagues to actively build a more competitive work environment while concentrating on the following three key drivers:

- Strengthening supervisors' leadership skills to establish a psychologically safe team culture and encourage active innovation
- Enhancing internal development by offering more diverse and rich learning resources, combined with employee development needs
- Actively exploring more non-monetary, diversified means of recognition to enhance employee engagement and satisfaction and further promote talent stability

In 2025, TSMC launched its culture refresh program 2.0, deeply integrating the Company's core values into key stages of the employee experience lifecycle, including talent sourcing, recruitment, onboarding, development, and retention. To achieve this, TSMC selected 16 culture ambassadors and redesigned training programs for new hires and newly appointed managers, aiming to deepen employees' understanding of and identification with TSMC's core values.

As of 2025, TSMC has conducted over 500 culture workshops globally. In 2025, a special focus was placed on JASM, where six culture workshops were successfully held. These efforts fostered cross-regional and cross-generational consensus on the Company's core values, built internal cultural literacy, and attracted and retained more like-minded talent. Moving forward, TSMC will continue to advance and refine its global cultural strategy and blueprint, aiming to comprehensively enhance the sense of belonging and identification with the corporate culture among all employees at TSMC and its global subsidiaries.

TSMC's turnover rate was 2.9% in 2025 compared to 3.5% in 2024, both within the healthy range of less than 10% (based on Willis Towers Watson's high performance employee experience or HPEX model).

5.6.11 Retirement Policy

TSMC has a statutory defined benefit plan and a supervisory committee of labor retirement reserve according to the Labor Standards Act, and also a statutory defined contribution plan according to Labor Pension Act, which became effective in 2005. For each region, TSMC has also established pension plans according to local standards and regulations. The previously mentioned supervisory committee not only holds quarterly meetings but also supervises affairs in connection with labor's retirement reserve fund. To meet legal requirements for financial disclosure and ensure sufficient funding levels, TSMC makes contributions based on statutory requirements and also engages an actuarial consulting firm to assess the valuation of the defined benefit plan. Please refer to pages 47 to 50 of TSMC's consolidated financial statements for details. Thanks to the Company's sound financial condition, it is able to ensure the future viability of employee retirement benefits and solid pension contributions and payments, all of which incentivize employees to make long-term career plans with and further deepen their commitment to TSMC.

5.7 Material Contracts

TSMC is not currently a party to any material contracts, other than those entered into in the ordinary course of its business. The Company's "Significant Contingent Liabilities and Unrecognized Commitments" are disclosed in our company's consolidated financial statements on the Market Observation Post System (MOPS).
Link to MOPS: https://mops.twse.com.tw/mops/#/web/hom