5. Operational Highlights

5.1 Business Activities

5.1.1 Business Scope

As the founder and a leader of the dedicated semiconductor foundry segment, TSMC has built its reputation by offering advanced and specialty wafer production processes and unparalleled manufacturing efficiency. TSMC strives to provide the best overall value to its customers, and the success of TSMC's business is manifested in the success of its customers.

TSMC provides a full range of integrated semiconductor foundry services that fulfill the increasing variety of customer needs. In the process, it has experienced strong growth by building close relationships with customers. Semiconductor suppliers from around the world trust TSMC with their manufacturing needs, thanks to its unique integration of cutting-edge process technologies, pioneering design services, manufacturing productivity and product quality.

In May 2009, TSMC established the New Businesses organization to explore non-foundry related business opportunities. In August 2011, the New Businesses organization was formally separated from the main TSMC organization as two subsidiaries, TSMC Solid State Lighting Ltd. and TSMC Solar Ltd., responsible for solid state lighting and solar business activities, respectively.

5.1.2 Customer Applications

TSMC manufactured more than 8,600 different products for over 440 different customers in 2013. These chips are used across the entire spectrum of electronic applications, including computers and peripherals, information appliances, wired and wireless communications systems, automotive and industrial equipment, consumer electronics such as DVDs, digital TVs, game consoles, digital still cameras (DSCs), and many other applications.

The rapid evolution of end products drives our customers to utilize TSMC's innovative technologies and services, while at the same time spurring TSMC's own development of technology. As always, success depends on leading rather than following industry trends.

TSMC manufactured over 8,600 products for over 440 customers in 2013. TSMC significantly outgrew the semiconductor market in 25 of the last 27 years since its founding.

5.1.3 Consolidated Shipments and Net Revenue in 2013 and 2012

Unit: Shipments (8-inch equivalent wafers) / Net Revenue (NT$ thousands)

		2013		2012	
		Shipments	Net Revenue	Shipments	Net Revenue
Wafer	Domestic (Note 1)	2,810,456	79,982,833	2,392,978	65,782,349
	Export	12,855,511	480,702,380	11,651,318	397,188,087
Others (Note 2)	Domestic (Note 1)	N/A	5,118,245	N/A	4,764,100
	Export	N/A	31,220,739	N/A	39,010,698
Total	Domestic (Note 1)	2,810,456	85,101,078	2,392,978	70,546,449
	Export	12,855,511	511,923,119	11,651,318	436,198,785

Note 1: Domestic means sales to Taiwan.
Note 2: Others majorly include revenue associated with mask making, design, and royalty income.

5.1.4 Production in 2013 and 2012

Unit: Capacity / Output (8-inch equivalent wafers) / Amount (NT$ thousands)

	Wafers		
Year	Capacity	Output	Amount
2013	16,446,779	15,197,701	301,305,826
2012	14,832,671	13,643,678	267,104,646

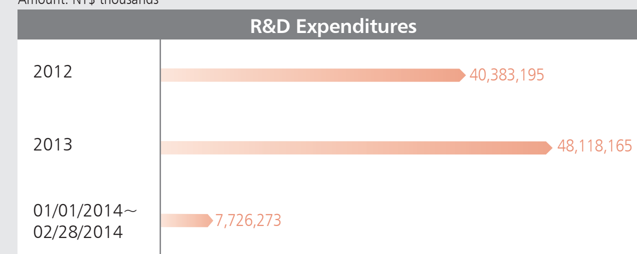
Note: Starting 2013, TSMC no longer includes SSMC's capacity in this capacity tables.

5.2 Technology Leadership

5.2.1 R&D Organization and Investment

In 2013, TSMC continued to invest in R&D with total R&D expenditure amounting to 8% of revenue, a level that equals or exceeds the R&D investment of many other high technology leaders. Along with the increase in budget, R&D staffing increased by 11%.

Amount: NT$ thousands



TSMC recognizes that the technology challenge required to extend Moore's Law, the business law behind CMOS scaling, is becoming increasingly complex. The efforts of the R&D organization are focused on enabling the Company to continuously offer its customers first-to-market, leading edge technologies and design solutions that contribute to their product success in today's complex and challenging market environment. In 2013 the R&D organization met these challenges by introducing into manufacture the industry-leading 20nm technology. The 16nm technology, which is the first integrated technology platform to make use of 3D FinFET transistors, has also met its development goals and is now in risk production. The R&D organization continues to strengthen the pipeline of technology innovations that are required to maintain technology leadership. The 10nm technology advanced development was completed, and entered full development, while the 7nm technology is in the early development stage.

In addition to CMOS logic, TSMC conducts research and development on a wide range of other semiconductor technologies that provide the functionality our customers require for mobile SoC and other applications. Highlights achieved in 2013 include: production ramp of the CoWoS™ (Chip on Wafer on Substrate) 3D packaging technology; extension of the 28nm technology for RF and embedded flash technologies; the first industry introduction of the BCD power technology into a 12-inch fab environment and, manufacturing readiness of TSMC's first wide band gap Gallium Nitride (GaN) semiconductor technology for high frequency power applications.

TSMC maintains a network of important external R&D partnerships and alliances with world-class research institutions such as IMEC, the respected European R&D consortium, where TSMC is a core partner. TSMC also provides funding for nanotechnology research at leading universities worldwide to promote innovation and the advancement of nanoelectronic technology. In 2013, TSMC announced the formation of collaborative research centers with National Taiwan University and National Chiao Tung University in Taiwan, and anticipates announcing the establishment of additional research centers in Taiwan in 2014.

5.2.2 R&D Accomplishments in 2013

R&D Highlights

- **28nm Technology**

TSMC delivered the world's first 28nm High-k/Metal Gate triple gate oxide technology (28HPT). This technology provides 10% faster speed compared to the 28HPM technology while keeping the same leakage power. 28HPT is qualified for production in both Fab 12 and Fab 15 with equivalent yield to 28HPM.

- **20nm Technology**

TSMC's 20nm technology was successfully qualified for volume manufacture.

- **16nm Technology**

The 16nm technology features FinFET transistors with a third generation High-k/Metal Gate process, a fifth generation of transistor strain process, and advanced 193nm lithography. FinFET transistors offer substantial power reduction at the same chip performance compared to transistors built with the traditional planar structure, which is essential for advanced mobile applications. In 2013, the R&D organization successfully verified the process development test vehicle (TV1R), provided customers with version 1.0 design kits (design rules and SPICE models) and offered two public cyber shuttles. More than 10 customers and IP vendors took the shuttles and verified their IP. The 16nm technology has completed manufacturing qualification with good yield.

- **10nm Technology**

2013 saw the introduction of 10nm technology into development. The 10nm technology will offer substantial power reduction for the same chip performance compared to earlier technology generations. Development activities in 2014 will focus on manufacturing baseline process setup, yield learning, transistor performance improvement, and reliability evaluation. TSMC plans to enter 10nm risk production in 2015 and volume production in 2016.

- **Lithography**

2013 was a productive year in 16nm lithography development with the technology reaching the risk production stage. Several novel patterning techniques were developed for 48nm pitch Fin patterning. These techniques overcame the challenge of high aspect ratio topography of 3D device structures. Besides patterning challenges, defect reduction on the high aspect ratio topography also required special engineering efforts. Several key solutions were developed in 2013, such as improvement in tool and process recipe co-optimization, and enhanced defect-monitoring methodology. The development of optimum automation and Advanced Process Control systems, including enhanced tool control and stability, resulted in significant reduction of rework rate and cycle time, helping to drive faster learning in both defect reduction and yield improvement.

Several new techniques were introduced during 2013 to enable the successful launch of 10nm development. While the immersion lithography process will be extended to the 10nm node, the double patterning technique that was developed for the 20nm and 16nm nodes is insufficient to meet 10nm requirements. Multiple patterning becomes essential to enable high yield manufacturing. To further stretch the patterning capability of optical lithography, significant learning in material processing, image modeling, and defect control has been achieved to make the 10nm process viable.

In 2013, TSMC took delivery of a NXE3300 extreme ultraviolet (EUV) scanner, and exposed its first wafers after successful installation. While we see a clear advantage in process simplification by the use of EUV as opposed to multiple patterning with optical immersion lithography, insufficient power of the EUV light source is our major concern.

Multiple e-beam direct-write lithography (MEB DW) not only has the potential for economical imaging critical layers, but it also may offer cost reduction potential for non-critical layers and 450-mm wafers. It is being developed to meet the need of 7nm node imaging and beyond. A TSMC team from the design, CMOS, MEMS, and packaging areas is jointly developing and fabricating the digital pattern generation (DPG) module for the Reflective E-Beam Lithography (REBL) system of KLA-Tencor. The first DPG test chip, which was a collaborative effort between TSMC and KLA-Tencor, was taped out in the third quarter of 2013.

- **Mask Technology**

Mask technology is an integral part of our advanced lithography. In 2013, we completed the development of mask technology for the 16nm node and made solid progress on development for the 10nm node. In the meantime, continued progress is being made on the mask technology for EUV lithography. Working with suppliers, we continue to drive down counts of native defects on mask blanks. In addition TSMC continues to work with several industrial consortia in developing the infrastructure of EUV mask technology.

Integrated Interconnect and Packaging

- **3D IC**

TSMC achieved a new industry landmark in 2013 with the ramp up to volume production of a new turnkey system integration solution called CoWoS™. The CoWoS™ solution is integrated with TSMC's advanced silicon technologies to provide customers with alternatives for system level integration compared to the traditional SoC approach. The technology has passed customer product qualifications with 28nm FPGA products. At 20nm, development continues and we expect customer tape outs in the first half of 2014. We successfully demonstrated 3D IC stacking of an application processor and wide I/O DRAM in 28HPM technology through transistor stacking (TTS) TSV technology, and completed 16nm TSV process development.

• Advanced Package Development
TSMC offers a wide variety of lead-free flip chip packaging technologies. In 2013, TSMC qualified for manufacture at 20nm an innovative Bump-on-Trace (BoT) packaging technology with an ultra-fine pitch (80μm) copper (Cu) bump that is suitable for mobile/handheld devices. Additionally, lead-free flip chip packaging was enhanced for ultra large die size ($\geq$600mm^2) for high performance applications (GPU/CPU/FPGA/Networking Processor).

• Advanced Interconnect
Development of low resistance Cu and low capacitance dielectric continued to be the primary focus in 2013. At the 16nm node, a novel dielectric scheme has been developed that reduces the capacitance between copper lines. For the 10nm node and beyond, we have developed a new spacer-patterning scheme that allows copper line width and spacing to be reduced and minimizes signal delay. The effective resistivity of copper lines developed with these advanced processes is highly competitive and is lower than that projected by the International Technology Roadmap for Semiconductors (ITRS).

Advanced Transistor Research

The increased performance and lower power requirements of advanced logic technologies require constant innovation in transistor architecture and materials. TSMC is at the forefront of research in these areas, with particular focus on non-silicon channel materials such as germanium and III-V compounds because of their desirable performance and power characteristics. As an example of the progress being made in this area, our research team recently announced at the 2013 International Electron Devices Meeting world record-breaking transistor performance for both Germanium (Ge) channel PMOS FinFET and Indium Arsenide (InAs) (III-V) channel NMOS. New concepts of transistor structures employing innovative nanotechnology are also under intensive investigation.

Specialty Technologies

TSMC offers a broad mix of technologies to address the wide range of applications that customers are engaged in. The Company enhanced its SoC roadmap to address the needs of specialty applications in mixed-signal, RF markets, high voltage power management IC, high voltage IC's for display, MEMS and embedded memory.

• Mixed Signal/Radio Frequency (MS/RF) Technology
TSMC has successfully verified customer products in the 28nm technology for RF CMOS applications (28LP-RF) that are aimed at next generation RF transceivers (e.g. 4G LTE). Higher performance analog and RF solutions are also in development at the 20nm node. TSMC developed and transferred to manufacturing a first generation 0.18μm Complementary Bipolar Complementary MOS (CBCMOS) technology.

• Power IC/BCD Technology/Panel Drivers
TSMC released the 0.13BCD technology, the first BCD technology to be implemented in a 12-inch fab. The R&D team also completed development and qualified for manufacture the wide band gap material GaN in a high electron mobility transistor (HEMT) configuration for high power, high frequency applications. The 55HV technology was qualified targeting high quality mobile displays, while C015HV was released targeted at the large panel market. TSMC has also developed a 0.18μm HV embedded flash technology for touch panel applications.

• Micro-electromechanical Systems (MEMS) Technology
A variety of products were qualified for manufacturing ramp in 2013, including products aimed at: giga-level pixel display density; BioMEMS applications such human genome sequencing; second generation motion sensor products; and high-resolution noise cancellation microphones.

• Flash/Embedded Flash Technology
TSMC achieved several important milestones in embedded flash technologies. At the more mature 65nm/55nm node, NOR based cell technologies including 1-T cell and Split-Gate cell successfully completed customer qualification. At the 40nm node, the split-gate cell technology has been shipped for both automotive and consumer applications. Embedded flash development for the 28LP and 28HPM platforms is underway for low leakage applications such as smartcard, MCU and Automobile.

5.2.3 Technology Platform

TSMC provides our customers with advanced technology platforms that include the comprehensive design infrastructure required to optimize design productivity and cycle time. These include: design flows for electronic design automation (EDA); silicon-proven IP building blocks, such as libraries; and simulation and verification design kits, i.e., process design kits (PDK) and technology files.

To ensure the OIP ecosystem delivers to our customers the highest quality design experience with newly introduced technologies, TSMC has collaborated with our EDA partners to certify EDA tool readiness. In particular, since 16nm is the first FinFET technology for our customers, TSMC and ecosystem partners improved the tool certification process to cover point tool enhancement as well as integrated, cross-tool certification using an advanced CPU core as the vehicle (EDA tool certification results can be found on TSMC-Online).

Given the ever-increasing need for first-time silicon success and early time-to-market for highly integrated circuits, in 2013 TSMC also extended its IP quality program (TSMC9000) to allow IP audits to be performed either at TSMC or at TSMC-certified laboratories. The extended IP quality program currently includes standard interface IP such as MIPI, HDMI and LVDS. Further IP types will be included in the upcoming year. TSMC also donated its IP Tag format to the industry to extend IP quality tracking coverage beyond our IP Alliance partners. To help customers plan new product tape-outs incorporating TSMC certified IP, the OIP ecosystem now features a portal to connect customers to an ecosystem of more than 40 solution providers.

5.2.4 Design Enablement

TSMC's technology platforms provide a solid foundation for design enablement. Customers can design directly using the Company's internally developed IP and tools, or using those that are available via our OIP partners.

Tech File and PDK

TSMC provides a broad range of process design kits (PDK) for digital logic, mix-signal, radio frequency (RF), high-voltage driver, CMOS Image Sensor (CIS) and embedded flash technologies across a range of technology nodes from 0.5μm to 16nm. In addition, TSMC provides technology files for: DRC; LVS; RC extraction; automatic place and route; and a layout editor to ensure process technology information is accurately represented in EDA tools. There are more than 100,000 customer downloads of these files every year.

Library and IP

TSMC and its alliance partners offer our customers a rich portfolio of reusable IP, which are essential building blocks for many circuit designs. In 2013, over 60% of new tape-outs at TSMC adopted one or more libraries or IP from TSMC and/or our IP partners. In 2013, TSMC expanded its library and silicon IP portfolio to contain more than 6,300 items, a 16% increase over 2012.

Design Methodology and Flow

In 2013 TSMC addressed the critical design challenges associated with the new 16nm FinFET technology for digital and SoC applications, as well as 3D IC chip stacking technology by announcing the readiness of reference flows through our Open Innovation Platform® (OIP) collaboration.

The 16nm reference flow features FinFET-specific design solutions and methodologies for performance, power, and area optimization. The flow covers place-and-route, RC extraction, timing analysis, electromigration, IR-drop, and physical verification. In addition, it includes analysis capability for layout-dependent-effects (LDE) and voltage-dependent rule checking (VDRC) to improve custom design accuracy and productivity.

The 3D IC Reference Flow is an extension of our previously announced CoWoS™ Reference Flow that addresses true 3D chip stacking. The 3D IC flow provides a complete solution for through-silicon via (TSV) modeling, power integrity, thermal analysis, chip-package-board switching noise analysis, and design for test (DFT) for memory integration through a Wide IO interface. These tools allow customers to fully explore the new system integration opportunities made possible by 3D IC technology.

5.2.5 Intellectual Property

A strong portfolio of intellectual property rights strengthens TSMC's technology leadership and protects our advanced and leading edge technologies. In 2013, TSMC received a record breaking 940 U.S. patents, as well as 500+ issued patents in Taiwan and the PRC, and other patents issued in various other countries. In 2013, TSMC ranked #35 in the "Top 50" U.S. patent grants. TSMC's patent portfolio now exceeds 20,000 patents worldwide (including patent applications in queue). We continue to implement a unified strategic plan for TSMC's intellectual capital management. Strategic considerations and close alignment with the business objectives drive the timely creation, management and use of our intellectual property.

At TSMC, we have built a process to extract value from our intellectual property by aligning our intellectual property strategy with our R&D, operations, business objectives, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities.

We have worked continuously to improve the quality of our intellectual property portfolio and to reduce the costs of maintaining it. We plan to continue investing in our intellectual property portfolio and intellectual property management system to ensure that we protect our technology leadership and receive maximum business value from our intellectual property rights.

5.2.6 TSMC University Collaboration Programs

TSMC University Research Centers in Taiwan

TSMC has significantly expanded its interaction with universities in Taiwan with the establishment of several new research centers located at the nation's most prestigious universities. The mission of these centers is twofold: to increase the number of highly qualified students who are suitable for employment at TSMC, and to inspire university professors to initiate research programs that focus on the frontiers of semiconductor device, process and materials technology; semiconductor manufacturing and engineering science; and specialty technologies of relevance to the semiconductor industry. Two of these research centers were established in 2013 at National Taiwan University and National Chiao Tung University, and two additional centers will be established at National Cheng Kung University and

National Tsing Hua University in 2014. These centers are funded jointly by governmental agencies together with a commitment from TSMC of several hundred million Taiwan dollars and in-kind university shuttles. In 2013, about three hundred high caliber students across Electronics, Physics, Materials Engineering, Chemistry, Chemical Engineering and Mechanical Engineering disciplines joined the research centers.

TSMC University Shuttle Program

The TSMC University Shuttle Program was established to provide professors at leading research universities worldwide with access to the advanced silicon process technologies that are needed to research and develop innovative circuit design concepts. This program links motivated professors and graduate students with enthusiastic managers at TSMC with the goals of promoting excellence in the development of advanced silicon design technologies, and the nurturing of new generations of engineering talent in the semiconductor field.

The program provides access to silicon process technologies including the 65nm and 40nm nodes for digital, analog/mixed-signal circuits and RF design, and the 0.11μm/0.18μm process nodes for micro-electromechanical system designs. Select research projects utilize the 28nm technology node. Participants in the TSMC University Shuttle Program include major university research groups in the U.S.: M.I.T.; Stanford University; UC Berkeley; UCLA; University of Texas at Austin; and University of Michigan. In Taiwan, participants are: National Taiwan University; National Chiao Tung University; and National Tsing Hua University. Other participants include: Tsing Hua University in Beijing; The Hong Kong University of Science and Technology; and Singapore's Nanyang Technological University.

TSMC's University Shuttle Program participants recognize the importance of the program in allowing their graduate students to implement exciting designs ranging from: low-power memories; analog-to-digital converters; and advanced radio-frequency and mixed-signal bio-medical systems. This is truly a "win-win" collaboration. In 2013, TSMC received specific letters of appreciation from professors at M.I.T., Stanford University, UC Berkeley, UCLA, University of Michigan, National Taiwan University and National Chiao Tung University.

5.2.7 Future R&D Plans

In light of the significant accomplishments of TSMC's advanced technologies in 2013, the Company plans to continue to grow its R&D investments. The Company plans to reinforce its exploratory development work on new transistors and technologies, such as 3D structures, strained-layer CMOS, high mobility materials and novel 3D IC devices. These studies of the fundamental physics of nanometer CMOS transistors are core aspects of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to ensure our continued industry leadership at the 28nm and 20nm nodes and to extend our leadership to the 10nm and 7nm nodes. One of TSMC's goals is to extend Moore's Law through both innovative in-house work and by collaborating with industry leaders and academia. We seek to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC intends to continue working closely with international consortia and lithography equipment suppliers to ensure the timely development of 193nm high-NA scanner technology, EUV lithography, and multiple- e-beam direct-write technologies. These technologies are increasingly important to TSMC's process development efforts at the 10nm, 7nm, and smaller nodes.

Similarly, TSMC continues to work with mask writing, inspection, and repair equipment suppliers to develop viable mask-making technology to help ensure that the Company maintains its leadership position in mask quality and cycle time and continues to meet aggressive R&D, prototyping, and production requirements.

With a highly competent and dedicated R&D team and its unwavering commitment to innovation, TSMC is confident of its ability to deliver the best and most cost-effective SoC technologies for its customers, thereby supporting the Company's business growth and profitability.

TSMC R&D Future Major Project Summary

Project Name	Description	Risk Production (Estimated Target Schedule)
10nm logic platform technology and applications	3rd generation FinFET technology for both digital and analog products	2015
7nm logic platform technology and applications	CMOS platform technology for SoC	2017
3D IC	Cost-effective solution with better form factor and performance for SIP	2014 ~ 2016
Next-generation lithography	EUV and multiple e-beam to extend Moore's Law	2014 ~ 2019
Long-term research	Special SoC technology (including new NVM, MEMS, RF, analog) and 5nm transistors	2014 ~ 2019

The above plans accounted for roughly 70% of the total R&D budget in 2014. The total R&D budget is currently estimated to be around 8% of 2014 revenue.

5.3 Manufacturing Excellence

5.3.1 GIGAFAB™ Facilities

TSMC's 12-inch fabs are a key part of its manufacturing strategy. TSMC currently operates three 12-inch GIGAFAB™ facilities – Fab 12, Fab 14, and Fab 15 – the combined capacity of which reached 4,619,000 12-inch wafers in 2013. Production within these three facilities supports 0.13μm, 90nm, 65nm, 40nm, 28nm, and 20nm process technologies, and their sub-nodes. Part of the capacity is reserved for research and development work and currently supports 16nm, 10nm and beyond technology development. TSMC has developed a centralized fab manufacturing management for the customers' benefit of consistent quality and reliability performance, greater flexibility of demand fluctuations, faster yield learning and time-to-volume, and minimized costly product re-qualification. It enabled Fab 15 to fast ramp 28nm capacity from 50,000 to around 100,000 wafers output per month in 2013 to satisfy customers' demand.

5.3.2 Engineering Performance Optimization

Highly sophisticated information technology (IT) solutions, such as advanced equipment control, fault detection and diagnosis, engineering big data mining, and centralized operation platforms, are implemented to optimize TSMC equipment, process and yield performance. They also improve production efficiency, effectiveness, and engineering capability via information integration, workflow optimization and automation.

Advanced analytical methods identify critical equipment and process parameters that are linked to device performance. Methodologies such as virtual metrology, yield dissection and management integrate Advanced Process Control (APC), Fault Detection Classification (FDC), Statistical Process Control (SPC), and Circuit Probe data in order to optimize equipment performance to match device performance.

Accurate modeling and control at each process stage drives intelligent module loop control. The process control hierarchy dispatched via sophisticated computer-integrated manufacturing systems enables optimization from equipment to end product, which achieves precision and lean operation in a high product mix semiconductor manufacturing environment.

5.3.3 Precision and Lean Operations

TSMC's unique manufacturing infrastructure is tailored for a high product mix foundry environment. Following its commitment to manufacturing excellence, TSMC has equipped a sophisticated scheduling and dispatching system, implemented industry-leading automated materials handling systems, and employed Lean Manufacturing approaches to provide customers with on-time-delivery and best-in-class cycle time. Real-time equipment performance and productivity monitoring, analysis, diagnosis and control minimize production interruption and maximize cost effectiveness.

5.3.4 450mm Wafer Manufacturing Transition

TSMC joined the Global 450mm Consortium (G450C) located in the College of Nanoscale Science and Engineering (CNSE) of New York University at Albany, New York. The consortium includes five IC makers and CNSE (which represents New York State and provides the clean room facility), as well as key 450mm tool suppliers as associate members.

Currently, TSMC has 16 experienced employees working in the consortium. TSMC has assumed the Operation General Manager position in the consortium and commits to lead the industry for a cost-effective 450mm transition. The clean room of G450C in Albany has been ready for tool installation since the first quarter of 2013. Most of the tools will be installed by 2015.

Besides 450mm tool readiness, TSMC is also developing novel 450mm operations to bring the maximum value of semiconductor wafer fabrication to customers, including advanced quality and the most competitive cycle time in advanced technology. 450mm will be a new era of semiconductor manufacturing with new manufacturing capability advanced from today's leading edge technology.

5.3.5 Raw Materials and Supply Chain Risk Management

In 2013, TSMC continued Supply Chain Risk Management review meetings periodically with business teams to proactively identify and manage risk of supply capacity insufficiency and supply chain interruption. TSMC also worked with its suppliers to enhance the performance of quality, delivery, risk management, and to support green procurement, environmental protection and safety.

Raw Materials Supply

Major Materials	Major Suppliers	Market Status	Procurement Strategy
Raw Wafers	F.S.T. S.E.H. Siltronic SUMCO SunEdison	These five suppliers together provide over 90% of the world's wafer supply. Each supplier has multiple manufacturing sites in order to meet customer demand, including plants in North America, Asia, and Europe.	•TSMC's suppliers of silicon wafers are required to pass stringent quality certification procedures. •TSMC procures wafers from multiple sources to ensure adequate supplies for volume manufacturing and to appropriately manage supply risk. •TSMC maintains competitive price and service agreements with its wafer suppliers, and, when necessary, enters into strategic and collaborative agreements with key suppliers. •TSMC regularly reviews the quality, delivery, cost and service performance of its wafer suppliers. The results of these reviews are incorporated into TSMC's subsequent purchasing decisions. •A periodic audit of each wafer supplier's quality assurance systems ensures that TSMC can maintain the highest quality in its own products.
Chemicals	Air Products ATMI BASF Dow SAFC KANTO-PPC MGC	These seven companies are the major suppliers for bulk and specialty chemicals.	•Most suppliers have relocated many of their operations closer to TSMC's major manufacturing facilities, thereby significantly improving procurement logistics. •The suppliers' products are regularly reviewed to ensure that TSMC's specifications are met and product quality is satisfactory.
Litho Materials	AZ Dow JSR Nissan Shin-Etsu Chemical Sumitomo T.O.K.	These seven companies are the major suppliers for worldwide litho materials.	•TSMC works closely with its suppliers to develop materials able to meet application and cost requirements. •TSMC and suppliers periodically conducts improvement programs of their quality, delivery, sustainability and green policy, to ensure continuous progress of TSMC's supply chain.
Gases	Air Liquide Air Products Linde Taiyo Nippon Sanso	These four companies are the major suppliers of specialty gases.	•The majority of the four suppliers are located in different geographic locations, minimizing supply risk to TSMC. •TSMC conducts periodic audits of the suppliers' quality assurance systems to ensure that they meet TSMC's standards.
Slurry, Pad, Disk	Air Products Asahi Glass Cabot Microelectronics Dow Chemical Fujifilm Planar Solutions Fujimi Hitachi Chemical Kinik 3M	These nine companies are the major suppliers for CMP materials.	•TSMC works closely with its suppliers to develop materials able to meet application and cost requirements. •TSMC and suppliers periodically conducts improvement programs of their quality, delivery, sustainability and green policy, to ensure continuous progress of TSMC's supply chain.

Suppliers Accounted for at Least 10% of Annual Consolidated Net Procurement

Unit: NT$ thousands

Supplier	2013			2012		
	Procurement Amount	As % of 2013 Total Net Procurement	Relation to TSMC	Procurement Amount	As % of 2012 Total Net Procurement	Relation to TSMC
VIS	6,993,964	17%	Investee accounted for using equity method	4,475,674	11%	Investee accounted for using equity method
Company A	4,925,966	12%	None	6,708,942	16%	None
Company B	4,812,417	11%	None	5,846,449	14%	None
Company C	4,401,215	11%	None	3,954,602	9%	None
Others	20,773,685	49%		20,394,725	50%	
Total Net Procurement	41,907,247	100%		41,380,392	100%	

5.3.6 Quality and Reliability

A characteristic of TSMC's industry reputation is its commitment to providing customers with the best quality wafers and service for their products. Quality and Reliability (Q&R) services aim to achieve "quality on demand" to fulfill customers' needs regarding time-to-market, reliable quality, and market competition over a broad range of products.

Q&R technical services assist customers in the technology development and product design stage to design-in their product reliability requirements. Since 2008, Q&R has worked with R&D to successfully establish and implement new qualification methodology for High-k/Metal Gate (HKMG) as well as for FinFET structures in 2013. Q&R had been collaborating with SEMI, the Semiconductor Equipment and Material International, to establish an IC Quality Committee since May 2012 in order to enhance product quality of the semiconductor supply chain. For backend technology development, Q&R worked with R&D and the Backend Technology and Service Division to complete the Cu Bump technology development and production transfer of both CuBoL (Copper Bump on Lead) and CuBoT (Copper Bump on Trace) as lead free bump solutions for fine bump pitch products. To extend product package reliability validation, Q&R established in-house system-level temperature cycling, bending, drop and vibration test capabilities in 2013.

In 2013, Q&R completed a new audit of incoming material suppliers for advanced technology. Q&R also implemented innovative statistical matching methodologies to achieve the goal of enlarging the manufacturing window with better quality control. The scope of the methodology includes facility, metrology and process tools, wafer acceptance test (WAT) data and reliability performance. Since 2011, Q&R tightened the post-fab outgoing visual inspection criteria for wafer quality improvement to AQL 0.4% from AQL 0.65%.

To sustain production quality, and to minimize risk to customers when deviations occur, manufacturing quality monitoring and event management span all critical stages – from raw material supply, mask making, and real-time in-process monitoring, to bumping, wafer sort and reliability performance. Advanced failure and materials analysis techniques are also developed and effectively deployed in process development, customer product development and product manufacturing. In recent years, due to continuous shrinking of device features, laboratory tools have been adapted to complement traditional metrology tools that have run into their physical limits. Furthermore, state-of-the-art materials analysis, chemical analysis and fault isolation equipment are continuously being added to support development activities of the 20nm, 16nm and 10nm technology nodes.

In compliance with the electronic industry's lead-free and green IC package policy, Q&R qualified and released lead-free bumping to satisfy customer demands, and made lead-free bump package possible for 0.13μm, 45nm, 40nm, 28nm and 20-SoC technology products by collaborating with the major outsource assembly and testing subcontractors. This enabled TSMC customers to introduce and ramp lead-free products with excellent assembly quality. In 2013, TSMC Q&R ramped wafer-level Chip Scale Package (CSP) to 21K per month and lead-free to 60K per month without major quality issues. For mainstream technologies, Q&R qualified ultra, extreme low leakage and high endurance embedded Flash IP, IPD (Integrated Passive Device), hybrid of Copper, and Copper-Aluminum technology with customers. Q&R continues to build reliability testing and monitoring to ensure excellent manufacturing quality of specialty technologies on automotive, high-voltage products, CMOS image sensors and embedded-Flash memory products.

TSMC Q&R is also responsible for leading the Company towards the ultimate goal of zero-defect production through the use of continuous improvement programs. Periodic customer feedback indicates that products shipped from TSMC have consistently met or exceeded their field quality and reliability requirements. In 2013, a third-party audit verified the effectiveness of the TSMC quality management system in compliance with ISO/TS 16949:2009 and IECQ QC 080000:2012 certificates requirements.

5.4 Customer Trust

5.4.1 Customers

TSMC's worldwide customers have diverse product specialties and excellent performance records in various segments of the semiconductor industry. Fabless customers include: Advanced Micro Devices, Inc., Broadcom Corporation, Marvell Semiconductor Inc., MediaTek Inc., NVIDIA Corporation, OmniVision Technologies and Qualcomm Inc. IDM customers include: Analog Devices Inc., STMicroelectronics and Texas Instruments Inc. etc.

Customer Service

TSMC believes that providing superior customer service is critical to enhancing customer satisfaction and loyalty, which is very important to retaining existing customers, attracting new customers, and strengthening customer relationships. With a dedicated customer service team as a main contact window for coordination and facilitation, TSMC strives to provide world-class, high-quality, efficient and professional services in design support, mask making, manufacturing, and backend to achieve optimum experience for our customers and, in return, to gain customer's trust and sustain Company profitability.

To facilitate customer interaction and information access on a real-time basis, TSMC-Online services offer a suite of web-based applications that provide a more active role in design, engineering, and logistics collaborations. Customers have 24-hour a day, seven-day-a-week access to critical information and are able to subscribe customized reports through TSMC-Online services. Design Collaboration focuses on content availability and accessibility, with close attention to complete, accurate, and current information at each level of the wafer design life cycle. Engineering Collaboration includes online access to engineering lots, wafer yields, wafer acceptance test (WAT) analysis, and quality reliability data. Logistics Collaboration provides access to data updated three times a day on any given wafer lot's status in order, fabrication, assembly and testing, and shipping.

Customer Satisfaction

To assess customer satisfaction and to ensure that of our customers' needs are appropriately understood, TSMC conducts an annual customer satisfaction survey (ACSS) with most active customers, either by web or interview, through an independent consultancy.

Complementary with the survey, quarterly business reviews (QBRs) are also conducted by the customer service team so that customers can give feedback to TSMC on a regular basis. Through both surveys and intensive interaction with customers by our account teams, TSMC is able to maintain close touch with customers for better service and collaboration.

Customer feedback is routinely reviewed and considered by executives and then developed into appropriate improvement plans, all-in-all becoming an integral part of the customer satisfaction process with a complete closed loop. TSMC has maintained a focus on customer survey data as one of our key indicators of corporate performance – not just of past performance, but also as a leading indicator of future performance. TSMC has acted on the belief that customer satisfaction leads to loyalty, and customer loyalty leads to higher levels of retention and expansion.

Customers Accounted for at Least 10% of Annual Consolidated Net Revenue

Unit: NT$ thousands

Customer	2013			2012		
	Net Revenue	As % of 2013 Total Net Revenue	Relation to TSMC	Net Revenue	As % of 2012 Total Net Revenue	Relation to TSMC
Customer A	130,563,982	22%	None	85,880,132	17%	None
Others	466,460,215	78%		420,865,102	83%	
Total Net Revenue	597,024,197	100%		506,745,234	100%	

5.4.2 Open Innovation Platform® (OIP) Initiative

Innovation has long been both an exciting and challenging proposition. Competition among semiconductor companies is becoming more active and intense in the face of increasing customer consolidation, and the commoditization of technology at more mature, conventional levels. Companies must find ways to continue innovating in order to prosper further. Companies innovating openly from the "outside in" as well as from the "inside out" accelerate innovation through active collaborations with external partners. This active collaboration of TSMC with external partners is known as Open Innovation. TSMC has adopted this path to innovate via the Open Innovation Platform® (OIP) initiative. OIP is a key part of the TSMC Grand Alliance.

The TSMC Open Innovation Platform® (OIP) initiative is a comprehensive design technology infrastructure that encompasses all critical IC implementation areas to reduce design barriers and improve first-time silicon success. OIP promotes the speedy implementation of innovation amongst the semiconductor design community and its ecosystem partners with TSMC's IP, design implementation and DFM capabilities, process technology and backend services.

A key element of OIP is a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that more efficiently empowers innovation throughout the supply chain and, in turn, drives the creation and sharing of newly created revenue and profits. TSMC's Active Accuracy Assurance (AAA) initiative is critical to OIP, providing the accuracy and quality required by the ecosystem interfaces and collaborative components.

TSMC's Open Innovation model brings together the innovative thinking of customers and partners under the common goal of shortening design time, minimizing time-to-volume and speeding time-to-market and, ultimately, time-to-revenue:

- The foundry segment's earliest and most comprehensive EDA certification program delivering timely design tool enhancement required by new process technologies; and
- The foundry segment's largest, most comprehensive and robust silicon-proven intellectual properties (IPs) and library portfolio; and
- Comprehensive design ecosystem alliance programs covering market-leading EDA, library, IPs, and design service partners.

TSMC's OIP Alliance consists of 28 electronic design automation (EDA) partners, 41 IP partners, and 25 design service partners. TSMC and its partners proactively work together, and engage much earlier and deeper than before in order to address mounting design challenges at advanced technology nodes. Through this early and intensive collaboration effort, TSMC OIP is able to deliver the needed design infrastructure with timely enhancement of EDA tools, early availability of critical IPs and quality design services when customers need them. This is critical to success for the customers to take full advantage of the process technologies once they reach production-ready maturity.

In October 2013, TSMC hosted an OIP Ecosystem Forum at the San Jose Convention Center in California, with keynote addresses from TSMC executives as well as OIP ecosystem partners. The forum was well attended by both customers and ecosystem partners and demonstrated the value of collaboration through OIP to nurture innovations.

TSMC's OIP Partner Management Portal facilitates communication with our ecosystem partners for efficient business productivity. This portal is designed with an intuitive interface and can be linked directly from TSMC-Online.

5.5 Employees

5.5.1 Human Capital

Human capital is one of the most important assets of TSMC. The Company is committed to providing quality jobs with good compensation, challenging work, and comfortable work environment for its employees, and it is dedicated to foster a dynamic and fun work environment. In 2013, TSMC was named the "Most Admired Company in Taiwan" by *CommonWealth Magazine* for the 17th consecutive year.

At the end of 2013, TSMC and its subsidiaries had over 40,483 employees worldwide, including 4,078 managers, 17,205 professionals, 3,236 assistants, and 15,964 technicians. The following table summarized TSMC workforce at the end of February, 2014:

TSMC Workforce Structure

		12/31/2012 (Note 1)	12/31/2013 (Note 2)	02/28/2014 (Note 2)
Job	Managers	3,865	4,078	4,105
	Professionals	15,844	17,205	17,225
	Assistant Engineer/Clerical	3,079	3,236	3,277
	Technician	16,479	15,964	16,156
Total		39,267	40,483	40,763
Gender	Male (%)	55.5%	57.5%	57.5%
	Female (%)	44.5%	42.5%	42.5%
Education	Ph.D.	3.6%	4.0%	4.0%
	Master's	34.5%	37.4%	37.2%
	Bachelor's	25.9%	25.8%	26.1%
	Other Higher Education	12.9%	11.9%	11.8%
	High School	23.1%	20.9%	20.8%
Average Age (years)		33.2	33.5	33.6
Average Years of Service (years)		6.2	6.6	6.7

Note 1: On a consolidated basis and includes employees of our non-wholly owned subsidiaries, Xintec Inc. and Mutual-Pak Technology Co., Ltd., since 2012.
Note 2: The data shown no longer includes Xintec Inc, as Xintec Inc. was deconsolidated in June 2013.

5.5.2 Recruitment

TSMC is an equal employment opportunity employer, and its practices center on the principles of open-and-fair recruitment. The Company evaluates all candidates according to their qualification as related to the requirement of each position, rather than race, gender, age, religion, nationality, or political affiliation.

Although facing a softer global economy, TSMC's continuous growth requires constant talent sourcing and recruitment activities to support its business. The Company recruited over 3,300 managers, professionals, and administrative staffs, as well as over 1,300 assistants and technicians in 2013.

In addition, the Company, through its University Program Office, established two university-level research centers in National Taiwan University (NTU) and National Chiao Tung University (NCTU) in 2013. Two other centers with National Cheng Kung University and National Tsing Hua University will be established in 2014. The mission of the centers is two-fold: to develop top graduate students for future employment and encourage selected academics to consolidate different research domains under one umbrella for more effective synergy. TSMC provides hundred of millions of NT dollars in seed money for leveraging funding from the National Science Council.

In 2013, the two centers in NTU and NCTU sponsored more than 50 faculty and 250 students across the fields of Electronics, Material Engineering, Physics, Chemistry, Chemical Engineering and Mechanical Engineering. These centers also help advance novel or innovative academic semiconductor research.

In order to cultivate a young talent pipeline for recruitment both locally and around the world, TSMC deploys a number of recruiting activities and university programs, including Joint Development Programs, University Shuttle Program, Summer Internship, Job Fairs in Taiwan, U.S., Singapore and India, as well as a series of Fresh Graduate Career Symposium for soon-to-be graduates.

5.5.3 People Development

TSMC is committed to cultivating a continuous and diversified learning environment. Under this mission, the Company initiated "TSMC Employee Training and Education Procedure" to ensure the Company's and individuals' development objectives can be achieved through internal and external training resources.

Based on the nature of the individual's job, work performance and career development path, the Company provides employees a comprehensive network of learning resources, including on-the-job training, classroom training, e-learning, coaching, mentoring, and job rotation.

For each employee, a tailor-made Individual Development Plan (IDP) is provided.

The Company provides employees with a wide range of on-site general, professional, and management training programs. In addition to engaging external experts as trainers, hundreds of TSMC employees are trained as qualified instructors to deliver their valuable know-how in internal training courses. In 2013, TSMC conducted 1,549 internal training sessions, which translated to a company-wide total of nearly 890,000 training hours with the participation of over 530,000 attendees. Employees on average attended over 22 hours of training and the total training expenses reached NT$83 million.

TSMC's training programs include:

- New Employee Training: includes basic training and job orientation for new employees. Furthermore, newcomers' managers and the Company's well-established Buddy System are in place to support the newcomers in their assimilation process.
- General Training: refers to training required by government regulations and/or Company policies, as well as trainings on general subjects for all employees or employees of different job functions. Such training includes subjects of industry-specific safety, workplace health and safety, quality, fab emergency response, languages, and personal effectiveness.
- Professional/Functional Training: provides technical and professional training required by different functions within the Company. TSMC offers training courses on equipment engineering, process engineering, accounting, information technology, and so forth.
- Management Training: programs are tailored to the needs of managers at all levels, including new, experienced, and senior managers; optional courses are also available.
- Direct Labor (DL) Training: enables employees of the production line in acquiring the knowledge, skills and attitudes they need to perform their jobs well and to pass the certification for operating equipment. Training includes DL Skill Training, Technician "Train-the-Trainer" Training, and Manufacturing Leader Training.

Apart from internal training resources, our employees are also subsidized when taking external short-term courses, credit courses and degrees.

5.5.4 Compensation

TSMC provides a diversified compensation program that is competitive externally, fair internally, and adapted locally. TSMC upholds the philosophy of sharing wealth with employees in order to attract, retain, develop, motivate and reward talented employees. With excellent operating performance, employment at TSMC entitles employees to a comprehensive compensation and benefits program above the industry average.

TSMC's compensation program includes a monthly salary, an employee cash bonus based on quarterly business results, and employee profit sharing when the Company distributes its profit each year.

The purpose of the employee cash bonus and profit sharing programs is to reward employee contributions appropriately, to encourage employees to work consistently toward ensuring the success of TSMC, and to link employees' interests with those of TSMC's shareholders. The Company determines the amount of the cash bonus and profit sharing based on operating results and industry practice in the Republic of China. The amount and form of the employee cash bonus and profit sharing are determined by the Board of Directors based on the Compensation Committee's recommendation, and the employee profit sharing is subject to shareholders' approval at the Annual Shareholders' Meeting. Individual awards are based on each employee's job responsibility, contribution and performance.

In addition to providing employees of TSMC's overseas subsidiaries with a locally competitive base salary, the Company grants annual bonuses as a part of total compensation. The annual bonuses are granted in line with local regulations, market practices, and the overall operating performance of each subsidiary, to encourage employees' commitment and development within the Company.

5.5.5 Employee Satisfaction

TSMC is committed to providing quality jobs with good compensation, challenging work, and comfortable work environment for its employees, and it is dedicated to foster a dynamic and fun work environment. The Company encourages employees to maintain a healthy and well-balanced life, apart from their time spent working.

TSMC's commitment in providing employees with a sustainable career with its continuous growth, as well as its unceasing efforts as an advocate for employees' work-life balance, has earned it the aforementioned "Most Admired Company in Taiwan" awarded by *CommonWealth Magazine*.

To enrich employees' work experience, the Company continuously implements programs to enhance their well-being, benefit, recognition, rewards and communication. The various initiatives include the following:

Employee Benefit Programs

- Diverse employee welfare programs: including 77 hobby clubs, 52 speeches covering diverse topics (in 2013), Sports Day, and Family Day. In addition, holiday bonuses, marriage bonuses, condolence allowances and emergency subsidies are also available to cater for employees' needs.
- Convenient on-site services: cafeterias, dry-cleaning, convenience stores, travel, banking, housing, and commuting assistance are accessible for employees in the fabs.
- Comprehensive health enhancement programs: physical care and psychological consultation services. Five free counseling sessions are offered to TSMC employees on an annual basis, with extension available depending on the individual's needs. Other programs include weight control, medical check-up, smoking secession, exercise promotion campaign, massage service, abdominal and neck x-ray, female care, blood donation, liver disease prevention, as well as seminars to raise awareness of personal health.
- Premium Sports Center: a variety of workout facilities available to all employees and their families, as well as exercise sessions conducted by professional instructors.
- Flexible Preschool Service: the childcare service, operated to meet employees' work schedules, is available in a total of three fabs in Hsinchu and Tainan.

Employee Recognition

TSMC sponsors various internal award programs to recognize employees' outstanding achievement, both as a team or on the individual level. With these award programs, TSMC aims to encourage employees' sustainable development that in turn adds to the Company's competitive advantage.

The award programs include:

- TSMC Medal of Honor, presented exclusively by the Chairman, recognizes those who contribute to the Company's business performance significantly.
- TSMC Academy recognizes outstanding TSMC scientists and engineers whose individual technical capabilities make significant contributions to the Company.
- Outstanding Engineer Award for each fab and Total Quality Excellence Award recognize employees' continuous efforts in creating value for the Company.
- Service Award represents TSMC's appreciation toward senior employees' dedication and commitment to the Company.
- Excellent Instructor Award praises the outstanding performance and contribution of the Company's internal instructors in training courses for employees.

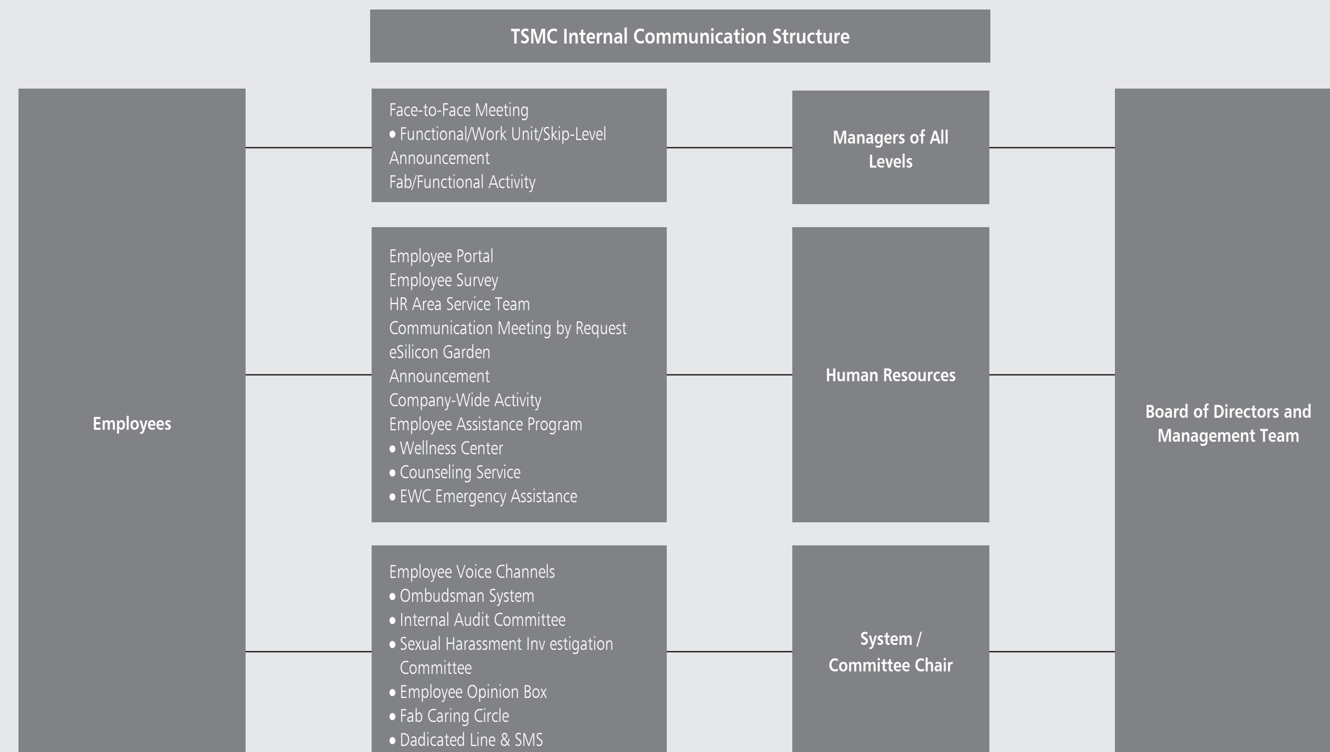
In 2013, TSMC employees continued to be recognized through a host of prestigious external awards, including National Outstanding Managers Award, Outstanding Young Engineer Award, National Model Worker Award, and National Industrial Innovation Award.

Employee Communication

TSMC values two-way communication and is committed to keeping the communication channels between the management level and their subordinates, as well as among peers, open and transparent. To ensure that employees' opinions and voices are heard, and their issues are addressed effectively, impartial submission mechanisms, including quarterly labor-management communication meetings, are in place to provide timely support. Our continuous efforts lie in reinforcing mutual and timely employee communication, based on multiple channels and platforms, which in turn fosters harmonious labor relations and creates a win-win situation for the Company and the employees. In 2013 and as of the date of this Annual Report, there had been no loss resulting from labor disputes.

A host of two-way communication channels are leveraged to maintain the unobstructed flow of information between the managers and the employees, including:

- Regular communication meetings are held for the various levels of managers and employees.
- Periodic employee satisfaction surveys are conducted, with follow-up actions based on the survey findings.
- The corporate intranet, *myTSMC*: the website features Chairman's Talk, corporate messages, Executive interviews, and other activities of interest to employees.
- *eSilicon Garden*: the website hosting TSMC's internal electronic publication is updated on a bi-weekly basis with inspirational content featuring outstanding teams and individuals, as well as major activities of the Company.
- Complaints regarding major management, financial, and auditing issues are handled by the following channels with high level of confidentiality:
  - The independent Audit Committee; and
  - Ombudsman system led by an appointed Vice President.
- Employee Opinion Box provides a channel for employees to express their opinions regarding their work and the overall work environment.
- Fab Caring Circle in each fab takes care of the issues related to employees' work and personal life. In 2013, the system dedicated mainly to the direct labors (DL) of the Company won the CSR Award presented by *GlobalView Magazine* with its quality and effective services.



5.5.6 Retention

From the employee's initial adaptation to professional and career development, TSMC works proactively to retain outstanding employees through good compensation and through an innovative, challenging and fun work environment. All these efforts contributed to a healthy turnover rate of 5.3% for 2013.

5.5.7 Retirement Policy

TSMC's retirement policy is set according to the Labor Standards Act and Labor Pension Act of the Republic of China. With the Company's sound financial system, TSMC ensures employees a solid pension contribution and payments, which encourages employees to set long-term career plans and raises their commitment to TSMC.

5.6 Material Contracts

Shareholders Agreement

Term of Agreement:
Effective as of 03/30/1999 and may be terminated as provided in the agreement
Contracting Parties:
Koninklijke Philips Electronics N.V. (Philips) and EDB Investments Pte Ltd. (EDBI)
(In September 2006, Philips assigned its rights and obligations under this agreement to Philips Semiconductors International B.V. which has now been renamed NXP B.V. In November 2006, NXP B.V. and TSMC purchased all SSMC shares owned by EDBI; EDBI is no longer a contracting party to this agreement.)
Summary:
TSMC, Philips and EDBI had formed a Singapore joint venture "Systems on Silicon Manufacturing Company Pte Ltd." (SSMC) for providing semiconductor foundry services. Philips Semiconductor (now NXP B.V.) and TSMC are committed to purchasing a certain percentage of SSMC's capacity.

Technology Cooperation Agreement

Term of Agreement:
03/30/1999 - 03/29/2004, automatically renewable for successive five-year terms until and unless either party gives written notice to terminate one year before the end of then existing term
Contracting Party:
Systems on Silicon Manufacturing Company Pte Ltd. (SSMC)
Summary:
TSMC agreed to transfer certain process technologies to SSMC, and SSMC agreed to pay TSMC a certain percentage of the net selling price of SSMC products.

Patent License Agreement

Term of Agreement:
12/20/2007 - 12/31/2017
Contracting Party:
A multinational company
Summary:
The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting company.

Manufacturing, License, and Technology Transfer Agreement

Term of Agreement:
04/01/2004 - 03/31/2006, automatically renewable for successive one-year terms until and unless both parties decide otherwise by mutual consent in writing
Contracting Party:
Vanguard International Semiconductor Corporation (VIS)
Summary:
VIS reserves certain capacity to manufacture TSMC products on mutually agreed terms. TSMC may also transfer certain technologies to VIS, for which it will in return receive royalties from VIS.

Investment Agreement and Shareholder Agreement

Term of Investment Agreement:
Effective as of 08/05/2012
Term of Shareholder Agreement:
Effective as of 10/31/2012 and may be terminated as provided in the agreement
Contracting Party:
ASML Holding N.V. (ASML)
Summary:
TSMC joined the Customer Co-Investment Program of ASML Holding N.V. (ASML) and entered into the investment agreement and shareholder agreement. The agreements include an investment of EUR837,815,664 by TSMC Global to acquire a non-voting 5% in ASML's equity with a lock-up period of 2.5 years.

Research and Development Funding Agreement

Term of Agreement:
10/31/2012 - 12/31/2017
Contracting Party:
ASML Holding N.V. (ASML)
Summary:
TSMC shall provide EUR276 million to ASML's research and development programs from 2013 to 2017.

Note: TSMC is not currently party to any other material contract, other than contracts entered into in the ordinary course of its business. The Company's "*Significant Contingent Liabilities and Unrecognized Commitments*" are disclosed in Annual Report (II), Financial Information, page 51.