5.1.3 Unconsolidated Shipments and Gross Sales in 2010 and 2009

Unit: Shipments (8-inch equivalent wafers) / Gross Sales (NT$ thousands)

		2010		2009	
		Shipments	Gross Sales	Shipments	Gross Sales
Wafer	Domestic	2,132,697	51,312,831	1,495,305	38,538,370
	Export	9,688,352	340,474,577	6,194,167	238,090,692
Package	Domestic	0	0	3	487
	Export	23,550	963,427	35,467	1,384,580
Other	Domestic	20,278	3,974,831	17,597	3,272,217
	Export	53,137	21,940,782	42,979	18,184,868
Total	Domestic	2,152,975	55,287,662	1,512,905	41,811,074
	Export	9,765,039	363,378,786	6,272,613	257,660,140

5.1.4 Production in 2010 and 2009

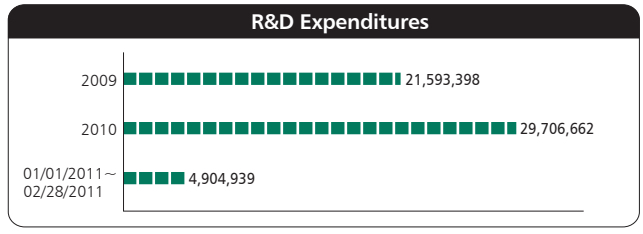
Unit:Capacity / Output (8-inch equivalent wafers) / Amount (NT$ thousands)

	Wafers		
Year	Capacity	Output	Amount
2010	11,328,601	11,806,566	199,376,792
2009	9,954,558	7,582,664	150,572,709

5.2 Technology Leadership

5.2.1 R&D Organization and Investment

(Amount: NT$ thousands)



TSMC expanded Research and Development in 2010 to further enhance one of its three strategic pillars: Technology Leadership. In 2010 the total R&D budget was 7% of total revenue. This level of R&D investment is equal to or more than that of many leading edge technology companies. Along with the budget increase, the R&D organization increased staffing by over 17%.

TSMC recognizes that the technology challenge required to extend Moore's Law, the business law behind CMOS scaling, is getting increasingly difficult. Dr. Shang-yi Chiang, TSMC Senior Vice President of R&D brings his rich industry experience to lead the strengthening of the R&D team and to navigate through the technological and competitive challenges ahead.

In 2010, TSMC offered the foundry segment's first 28nm technology. After intense work on ramping this technology, customers started to experience its benefits of stable and improved yield.

TSMC accelerated the development of advanced transistors, embedded memories, and copper (Cu)/low-K interconnect technologies. During 2010, the R&D organization once again proved its capabilities by offering a first-to-market 28nm high-K/metal gate (HKMG) foundry technology portfolio as well as establishing 20nm path-finding capability.

TSMC also expanded its external R&D partnerships and alliances with world-class research institutions. For example, TSMC is a core partner of IMEC, the respected European R&D consortium. TSMC also has a strategic agreement with IP provider to enable the development of physical IP through the advanced technology nodes. In addition, TSMC strengthened its collaborations with key partners on design-process optimization. TSMC provides funding for nanotechnology researches at major universities worldwide to promote innovation and the advancement of technology.

These research efforts enable the Company continuously to offer its customers the foundry-leading, first-to-market technology and design solutions that contribute to their product success in the complex and challenging market environment.

5.2.2 R&D Accomplishments in 2010

R&D Highlights

● 28nm Technology

TSMC continued to lead the foundry segment with the development of the most advanced logic technologies both with conventional as well as HKMG stacks. The high performance (28HP) platform is aimed at high-speed GPU and CPU applications. It also serves as the technology backbone for high-end FPGA and SoC application domains through additional device customization for leakage management. The low-leakage (28LP and 28HPL) technologies are designed to support low-cost mobile applications as well as low-end FPGA requirements.

With the improvement and development momentum, TSMC has continuously demonstrated breakthroughs in both 64Mb SRAM yield and technology reliability for all the 28nm technology family, including 28LP, 28HP and 28HPL. In addition, 28LP has completed the technology qualification in September 2010 and proved to be the first 28nm technology within the semiconductor and foundry industries ready for risk production. HKMG technology qualification is also under way.

In parallel, TSMC provided 28nm shuttle service program and successfully delivered proven and functional test-chips for both conventional SiON/poly and HKMG technologies. More than 10 shuttle services were offered in 2010, and more than 25 customers validated their test-chips and critical IPs with TSMC's 28nm technologies for various market segments, including GPU/CPU, FPGA and mobile applications.

● 20nm Technology

In 2010, TSMC continued to focus on 20nm technology path finding and development. To offer a leading-edge technology for both analog and digital application, the Company adopted the most advanced 193nm immersion and enhanced lithography process for smaller feature size. With the second generation of HKMG, more Si strain, and new device structure, the intrinsic transistor performance continues to ramp following Moore's Law. Meanwhile, external resistance can be effectively reduced and controlled by a specially designed process technique. The back end-of-line (BEOL) interconnect process features extreme low-K intermetal dielectric materials and copper metallization with the novel low-resistance scheme. The logic transistor and SRAM bit-cell offering, using the 20nm process, will cover high performance and System-on-Chip (SoC) application.

Development of 20nm technology will create superior gate density and chip performance. The cost and complexity of advanced technology will continue to escalate for customers. In 2010, TSMC provided process flow, design kits and intellectual property (IP) to help reduce foundry costs. TSMC's high-performance 20nm process will enter risk production in the third quarter of 2012, with volume production scheduled for the first quarter of 2013.

● Lithography

To overcome unprecedented low k_1 for imaging, state-of-the-art optical lithography resolution enhancement techniques, such as source-mask optimization and multiple patterning, have been implemented to achieve 2X the gate density of previous generation. Combined with an optimized etching technique and film stack, a nonlinear photoresist was introduced to achieve a 2.2nm line-width-roughness (LWR) on the switching gates to gain device performance.

The reticle for Test Vehicle 1 of the 20nm node was taped out in mid 2010 with an advanced super binary intensity mask (BIM) blank. The overlay control for inter- and intra-layers reached 6nm, a 25% gain from the previous generation. Moreover, with design rule optimization, the patterning technique of the active layer can be simplified from 3P2E to 2P2E, resulting in significant cost reduction.

Low-single-digit immersion defects for the 28nm node were achieved with track/material co-optimization that evolved from and is better than the previous generation. To deal with various product requirements, customized OPC was used. Low-cost solutions were developed for 0.11μm logics, multi-generation technologies, and special technologies such as eDRAM and CMOS Image Sensor (CIS).

For next generation lithography (NGL) technology development, a multiple e-beam maskless pre-Alpha tool installed in TSMC's fab has been demonstrating imaging with 110 beams and patterns of the 20nm node using e-beam proximity correction.

In early 2010, the Company announced the acquisition of a full-field extreme-ultraviolet (EUV) scanner from ASML Netherlands B.V. for the development of lithographic processes for devices of the 20nm node and below at TSMC's Fab 12 GIGAFAB™. TSMC has also made progress on demonstrating 20nm device processing with EUV lithography using the alpha demo tool located at our IMEC partner site.

● Mask Technology

Mask technology is an integral part of advanced lithography technology. TSMC has developed proprietary resolution-enhancement techniques (RET) that are co-optimized with our in-house mask-making technology. The Company integrates optical proximity correction (OPC) and scanner parameter optimization, and masks them together to provide a total solution in 193nm immersion lithography. TSMC's mask-making facilities feature state-of-the-art electron-beam mask writers, etchers, inspection, repair, verification, and metrology tools for production at 28nm and R&D at 20nm and beyond. TSMC continues to develop mask technologies for double patterning with 193nm immersion lithography and EUV lithography for applications to the 20nm generation and beyond and participates actively in developing the infrastructure for EUV mask-making. TSMC's strength in mask technology gives significant and unique benefits to its customers in terms of technical excellence, top quality, fast cycle time, and one-stop service.

Integrated Interconnect and Packaging

The Integrated Interconnect and Package Development Division (IIPD) was formed in late 2008 to develop and deliver an integrated technology solution combining advanced interconnect with packaging technology. The introduction of extreme low-K dielectric (ELK) in 45/40nm adds more challenges among many others to the given tasks. In 2010, the major focus was to resolve interconnect/package related bottlenecks and ensure smooth ramp of 45/40nm first-wave customers' products. Enhancement in Si backend/bump structure designs, and process optimization in bumping/assembly processes have paved the way for customers' products delivery with reliable quality. Customers including GPU and FPGA products are in volume production (with die size $>20\times20mm^2$).

● Advanced Interconnect

In 2010, TSMC continued to lead the foundry segment in demonstrating the lowest resistance/capacitance (RC) -delay interconnect technology in the segment, which is also compatible with advanced package technology.

Copper interconnect resistivity is trending up by generation node because of the size effect. To keep the RC performance for the advanced interconnect, TSMC has developed an extreme low resistance Cu interconnect solution for 28nm and beyond technology nodes. On the 28nm, we also improve effective resistivity of Cu lines to be significantly lower than that projected by the International Technology Roadmap for Semiconductors and demonstrate promising reliability performance.

● Advanced Package Development

To achieve "Green package" requirements and to follow the EU code for RoHS, the traditional tin-lead (Sn-Pb) based solder interconnect will be replaced by lead-free (Sn-Ag or Cu post) technology step-by-step. TSMC will continue to develop lead-free package technology (including die sizes, bump pitches, substrate types, etc.) and Fan-in Wafer Level Packaging (Fan-in WLP) for handheld/mobile devices/applications in 2011 to further enhance customers' product performance and competitiveness

● 3D IC

TSMC has committed to work with customers closely to develop cost-effective 3D IC system integration solutions using in-house proprietary through silicon via (TSV) and foundry compatible wafer-level-packaging (WLP) technologies. Our 3D System-in-Package (SiP) solution is a viable alternative for many customers to realize their end product with the best cost and cycle time. TSMC delivers innovations to enable SiP design for the first time. It includes SiP package design, electrical analysis of package extraction, timing, signal integrity, IR drop, and thermal to physical verification of design rule check (DRC) and Layout Verification of Schematic (LVS). Such integrated solution for product realization will be made available to customers in 2012/13.

Advanced Transistor Research

Historically, transistor performance requirement follows different market segments: high performance applications, such as desk top computing; low-operating power applications, such as laptop computers and mobile internet devices; and low standby power applications, such as cell phones for long standby time. TSMC has been the technology leader in the low-operating power applications with G-family transistors and low standby power applications with LP family transistors. As low-operating power applications spread into the high performance domain, TSMC is embracing the challenge to retune our transistor offering to assure customers that they have the most competitive transistor offering from TSMC.

Spectrum of Technology

Beyond the highlights above, TSMC continued to develop a broad mix of new technologies. The Company accelerated its SoC roadmap, including embedded DRAM (eDRAM) and RF with earlier availability, higher integration and more variants.

● Embedded DRAM

Continued with TSMC leadership in eDRAM, in 2010 we started to ramp up early production of 40nm LP eDRAM for more efficient memory density and throughput required for bandwidth and graphic applications such as games and DTV. This will be followed by baseband and network applications, using the N40G base logic with 412MHz and 500MHz clock rate. Development also began on N28 eDRAM using HKMG logic as a base technology.

● Silicon Germanium BiCMOS Radio Frequency (RF) Technology

SeGi018: Upgraded TSMC SiGe-BiCMOS technology performance to tier-1 SiGe process specifications. For the moment, we are ahead of the ITRS roadmap targets.

● Mixed Signal/Radio Frequency (MS/RF) Technology

TSMC delivered a 28nm EM simulation base LC tank design package to facilitate high speed Serdes design. This approach successfully fulfilled requirements for different customized metal schemes in a significantly shorter time. In the category of More-than-Moore product enhancement, we developed IPD technology on high R substrate, and provided excellent inductor ($Q>50$) and precise MiM (C corner$<5\%$) for the RF-FEM (front-end module) segment.

Thin film Resistor: Demonstrated a close to zero TCR TFR which is key for high-precision ADC.

● Power IC/BCD Technology

In 2010, TSMC released a multiple-time re-programmable (MTP) non-volatile memory into the existing C025BCD power management IC technology. A one-time programmable (e-fuse) solution was qualified in 0.25u/5V and 0.18u/5V mixed signal technologies and their derivatives (BCD, HV). These features enable customers to trim critical analog characteristics at wafer, package or board level in a cost efficient manner (e-Fuse) or enhance the product functionality (MTP).

Besides continuing various BCD technology developments for DC-DC conversion, TSMC successfully delivered UHV (800V) technology that supports designs for energy-efficient lighting (CFL, LED, E-balaster) and mobile adaptors.

- Panel Driver Technology

In mobile device display drivers, TSMC released two new technologies in 2010: C011HV and N80HV. These technologies are targeted for high resolution displays in smart phones.

To meet more stringent standards in large panel displays (color depth and speed) for new TVs, such as 3D LCD TV, TSMC released two technologies in 2010.

- Microelecrtromechancial Systems (MEMS) Technology

There are several MEMS technologies for different applications in development at TSMC. In 2010, we worked with a customer to release a gyroscope device in production. We also demonstrated preliminary success in a DNA sequencing device, and made significant progress in our motion sensor platform technology development.

- CMOS Image Sensor Technology

In 2010, TSMC extended our leadership in back-side illumination (BSI) to enable our key customer to win more visible business with popular handheld products. At the same time, BSI wafer processing in 12" bulk-silicon also started risk production with the 65nm 8-megapixel product to be ramped up in early 2011, followed by many others.

TSMC also won the business for another leading CIS provider for 12" technology development, with wafer loading scheduled for 2012.

- Flash/Embedded Flash Technology

In 2010, TSMC delivered a refined low power, extremely low leakage 0.18μm Flash for microprocessor control unit (MCU) applications. The 90nm split gate technology has passed technology qualification. Three macros were qualified. One key customer has delivered Bluetooth engineering samples to their customers. Smart card IP is being qualified with several customers joining shuttle service for product prototyping.

TSMC has engaged with several IDM companies to co-develop embedded flash solutions for automotive, industrial and consumer applications. The technology foundation used includes 90nm, 65nm and 55nm, with the flash cells varying from floating gate and split-gate to hybrid.

5.2.3 Technology Platform

Modern IC designers need sophisticated design infrastructure to achieve acceptable productivity and cycle time. This includes design flow for electronic design automation (EDA), silicon proven building blocks such as libraries and IPs, simulation and verification design kits such as process design kit (PDK) and tech files. All these are built on top of the technology foundation, and each technology needs its own design infrastructure to be usable for designers. This is the concept of a technology platform.

Today's TSMC technology platforms reflect the culmination of years of work by TSMC and its alliance partners. In 2008, TSMC's Open Innovation Platform™ was launched to further enhance the Company's technology platforms, with additional deliverables added on in 2010. The Company unveiled an extension to its IP Alliance program in October to include Soft IP partners.

In April, TSMC announced the foundry segment's first Analog/Mixed Signal (AMS) Reference Flow, and the second revision of the Radio Frequency Reference Design Kit (RF RDK). The new AMS Reference Flow is TSMC's first custom design flow that targets leading edge 28nm design challenges, such as Layout Dependent Effects (LDE), Design For Manufacturing (DFM) and Sub-1V, to minimize design barriers and reduce iterations. AMS Reference Flow is a fully integrated multi-vendor program and part of an innovative design package.

The updated RDK provides a solution to common bottlenecks that designers encounter on a daily basis. RDK 2.0 includes step-by-step tutorials and setup scripts to facilitate users going through Circuit Sizing/Design Centering, a comprehensive EM design flow with TSMC PDK, and to analyze substrate noise coupling in RF circuits with TSMC qualified SNA tools.

After the debut of a series of interoperable data formats in iRCX, iDRC, iLVS and iPDK in 2009, TSMC demonstrated its strong commitment to industry users in 2010 with its industry-first iDRC & iLVS runsets in 40nm, and iPDKs in many TSMC advanced process nodes from 0.13μm to 28nm. Working with EDA partners, TSMC publishes quarterly reports for their qualified interoperable tools and versions.

The Soft IP Alliance program aims to improve soft IP readiness for advanced technology nodes and to drive earlier time-to-market. Soft IP has historically been process technology independent and, therefore, not optimized for power, performance and area considerations. Given the ever-increasing need of first-time silicon success and early time-to-market for highly integrated circuits, such as Systems-on-Chip (SoC), close technical collaboration between the foundry and the IP provider is imperative to emphasize this critical trade-off.

iRCX, an interoperable EDA data format, integrates all key process interconnect modeling data, which is increasingly important as chip designs in advanced technologies require detailed views of parasitic effects for the accurate evaluation of chip performance and power consumption. iRCX offers foundry interconnect model data for various applications across the board, covering not only parasitic RC tools at transistor & gate levels, but also the commonly-used tools for Electrical Magnetic (EM) Solver, Field Solver and ElectroMigration (EM)/Current (IR) Drop Analysis. EDA tools that support the iRCX format will be able to receive accurate interconnect modeling data from the iRCX files developed and supported by TSMC.

Executable physical verification runsets for interoperable design rule check (iDRC), interoperable density fill (iFill) and interoperable layout-versus-schematic (iLVS) in TSMC 40nm process technology were delivered to TSMC beta customers in 2010. Design rules for advanced process technologies are more complex and require detailed and accurate descriptions for correct chip layout creation and post-layout analyses. TSMC iDRC and iLVS formats, based on TSMC process requirements, unify process design rules specification and technology file generation, simplify data delivery, and ensure data integrity and interpretation. These are also the deliverables that represent TSMC's tight collaboration with its EDA partners and mutual customers.

TSMC iPDK unified data model on industry-standard OpenAccess database enables design reuse that is not possible with multiple proprietary PDKs and design databases among various EDA design platforms. It eliminates duplicate PDK development efforts, significantly reduces PDK development, validation and support costs across the design ecosystem, and promotes innovation in analog and full custom design. With a wide range of available iPDKs in TSMC process nodes and industry available EDA design platforms, users are now offered a higher degree of design flexibility in choosing the best tool features to fit their design needs.

To ensure OIP Ecosystem partners' compliance with TSMC new process requirements, TSMC works with partners to publish the "EDA Tool Qualification Report" on TSMC-Online, providing customers with an actively maintained status of individual EDA tools including DRC, LVS, RC extraction, Placement and Routing. The physical verification tool qualification report of DRC/LVS/RCX is updated on quarterly basis, and started to cover iDRC/iLVS/iRCX/iFill from 2010. Also new for Year 2010, routing qualification of 28nm was introduced as the design rule becomes Version 1.0.

In order to lower the barrier of technology adoption for customers, TSMC first introduced the Integrated Sign-Off Flow (ISF) in 65nm/55nm in 2009. ISF is a production proven design flow based on TSMC's internal design expertise accumulated over the years. ISF started to bear fruits in 2010, and enabled a large number of first time 65nm/55nm customers. ISF significantly reduced technology adoption gap in emerging markets such as China.

Entering its 10th year, the TSMC Reference Flow continues to anticipate customer needs in advanced design methodologies, and to serve the purpose of pipe-cleaning EDA tool capabilities. Traditionally the Reference Flow addresses design challenges in power, timing, and design for manufacturing. Reference Flow 11.0 incorporated new requirements associated with leading edge technologies, such as 28nm, and expanded into two new areas: 3D IC with TSV (through silicon via) and ESL system level design. The former supports heterogeneous integration of multiple dice and to achieve superior timing/power/form factor optimization, while the latter supports the trend of designers moving up to system level, enabling earlier and more accurate tradeoff with accurate TSMC PPA (power, performance and area).

5.2.4 Intellectual Property

A strong portfolio of intellectual property rights strengthens TSMC's technology leadership and protects our advanced and leading edge technologies. In 2010, TSMC received 434 U.S. patents, 173 Taiwanese patents, 180 PRC patents, and other patents issued in various other countries. TSMC's patent portfolio now exceeds 13,000 patents worldwide. We continue to implement a unified model for TSMC's intellectual capital management. Strategic considerations and close alignment with the business objectives drive the timely creation, management and use of our intellectual property.

At TSMC, we have built a process to extract value from our intellectual property by aligning our intellectual property strategy with our R&D, business objectives, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities.

We have worked continuously to improve the quality of our intellectual property portfolio and to reduce the costs of maintaining it. We plan to continue investing in our intellectual property portfolio and intellectual property management system to ensure that we protect our technology leadership and receive maximum business value from our intellectual property rights.

5.2.5 Future R&D Plans

Following the significant accomplishments of TSMC's advanced technologies in 2010, the Company plans to continue to grow its R&D investments. TSMC will further expand its 300mm R&D pilot line to speed up 28nm production ramp and 20nm development. The Company plans to reinforce its exploratory development work on new transistors and technologies, such as 3D structures, strained-layer CMOS, high mobility materials, novel 3D-IC devices with TSV, and interposer. These studies of the fundamental physics of nanometer CMOS transistors are core aspects of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to

ensure our continued industry leadership at the 28nm and 20nm nodes. One of TSMC's goals is to extend Moore's Law through innovative in-house work, as well as by collaborating with industry leaders and academia to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC will continue working closely with international consortia and photolithography equipment suppliers to ensure the timely development of 193nm high-NA scanner technology, EUV lithography, and massively parallel E-Beam direct-write technologies. These technologies are now fundamental to TSMC's process development efforts at the 20nm and 14nm nodes and beyond.

TSMC continues to work with mask inspection equipment suppliers to develop viable inspection techniques, a collaborative partnership to help ensure the Company maintains its leadership position in mask quality and cycle time and continue to meet aggressive R&D, prototyping and production requirements.

With a highly competent and dedicated R&D team, and unwavering commitment to innovation, TSMC is confident of its ability to deliver the best and most cost-effective SoC technologies for customers, and to support the Company's business growth and profitability.

TSMC R&D future major project summary:

Project Name	Description	Risk Production (Estimated Target Schedule)
28nm logic platform technology and applications	28nm technology for both digital and analog products	2010 - 2011
20nm logic platform technology and applications	Next-generation technology for both digital and analog products	2012
14nm logic platform technology and applications	Exploratory technology for both digital and analog products	2014
3D-IC	Cost-effective solution with better form factor and performance for SIP	2012 - 2013
Next-generation lithography	EUV and multiple E-Beam to extend Moore's Law	2011 - 2012
Long-term research	Special SoC technology (including new NVM, MEMS, RF, analog) and 14nm transistors	2012 - 2014

The above plans account for roughly 70% of the total corporate R&D budget in 2011, which is currently estimated to be around 7-8% of 2011 revenue.

5.3 Manufacturing Excellence

5.3.1 GIGAFAB™ Fabrications

TSMC's 12-inch fabs are a key part of its manufacturing strategy. TSMC currently operates two 12-inch GIGAFAB™ fabrication facilities – Fab 12 and Fab 14 – whose combined capacity reached 2,520,000 12-inch wafers in 2010. Production within these two facilities supports 0.13μm, 90nm, 65nm, 40nm, and 28nm process technologies, and their sub-nodes. Part of the capacity is reserved for research and development work and currently supports 20nm, 14nm and beyond technology development. A third GIGAFAB™ fabrication, Fab 15, located in Taichung's Central Taiwan Science Park, is on track for equipment move-in during the second quarter of 2011.

TSMC has developed a centralized fab manufacturing management for the customers' benefit of same quality and reliability performance, greater flexibility of demand fluctuations, faster yield learning and time-to-volume, and minimized costly product re-qualification.

5.3.2 Engineering Performance Optimization

Highly sophisticated information technology (IT) solutions, such as advanced equipment control and fault detection, are implemented to optimize TSMC equipment performance and improve production efficiency.

Advanced analytical methods identify critical equipment and process parameters that are linked to device performance. Methodologies such as virtual metrology and yield management integrate Advanced Process Control (APC), Fault Detection Classification (FDC), Statistical Process Control (SPC), and Circuit Probe data in order to optimize equipment performance to match device performance. Accurate modeling and control at each process stage drives intelligent module loop control.

The process control hierarchy dispatched via sophisticated computer-integrated manufacturing system enable optimization from equipment to end product, which achieves precision and lean operation in a high product-mix semiconductor manufacturing environment.