

5.1 Business Activities

5.1.1 Business Scope

TSMC's business scope is IC foundry and associated services. The Company excels in all aspects of its business, including semiconductor process technology research and development, wafer manufacturing, logistics management, capacity utilization, customer service, and associated services such as design services, mask manufacturing, wafer probing, in-house bumping and testing. TSMC strives to provide the best overall value to customers; the success of TSMC's business is manifested in the success of its customers.

5.1.2 Customer Applications

Over the past 20 years, more than 500 customers worldwide have relied on TSMC to manufacture chips that are used across the entire spectrum of electronic applications, including computers and peripherals, information appliances, wired and wireless communications systems, automotive and industrial equipment, consumer electronics such as DVDs, digital TVs, game consoles, digital still cameras (DSCs), and many other applications.

The rapid evolution of end products drives our customers to utilize TSMC's innovative technologies and services, while at the same time spurring TSMC's own development of technology. As always, success depends on leading rather than following industry trends.

5.1.3 Shipments and Gross Sales in 2007 and 2006

Unit: Shipments (8-inch equivalent wafers) /Gross Sales (NT\$ thousands)

		2007		2006	
		Shipments	Gross Sales	Shipments	Gross Sales
Wafer	Domestic	1,442,285	38,066,322	1,087,883	30,945,735
	Export	6,255,368	246,329,084	5,670,064	246,018,463
Package	Domestic	53	3,641	104	8,548
	Export	303,427	12,192,114	438,599	21,227,574
Other	Domestic	15,945	3,471,751	13,968	3,050,487
	Export	43,148	19,104,387	41,045	17,959,341
Total	Domestic	1,458,283	41,541,714	1,101,955	34,004,770
	Export	6,601,943	277,625,585	6,149,708	285,205,378

5.1.4 Production in 2007 and 2006

Unit: Capacity/Output (8-inch equivalent wafers) /Amount (NT\$ thousands)

Wafers			
Year	Capacity	Output	Amount
2007	8,289,788	7,861,951	164,625,063
2006	7,061,856	7,154,333	147,668,232

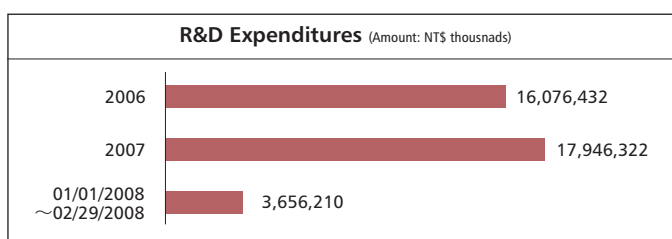
5.2 Technology Leadership

5.2.1 R&D Organization and Investment

TSMC increased its research and development investment and expanded its world-class R&D organization in 2007, strengthening its lead in providing best-in-class semiconductor technologies and design solutions to its customers. The Company also expanded its R&D in mainstream and derivative technologies, advanced CMOS and system-on-chip (SoC). R&D expenditure reached NT\$17.9 billion, while R&D staff grew by 14.5% during the same period. The Company will continue to invest significant amounts in research and development in 2008.

TSMC has accelerated its developments of transistor, memory, and interconnect technologies with a new R&D organization. During 2007, the R&D organization once again proved its value by providing a first-to-market portfolio of 45nm foundry technology as well as the industry's first 32nm capability. TSMC also expanded its external R&D partnerships and alliances with world-class research institutions. For example, TSMC is a core member of IMEC, the respected European CMOS R&D consortium. TSMC also has a partnership agreement with NXP, a semiconductor company with world-class technology, to conduct exploratory research and modeling in advanced CMOS, beyond CMOS, and special "more than Moore" technologies. In addition, TSMC has strengthened its collaborative research with key partners on design-process optimization. TSMC also continues to fund nanotechnology research at major universities worldwide to promote innovation and the advancement of technology.

These research efforts enable the Company to offer its customers industry-leading, first-to-market technology and design solutions, helping to ensure their product success in this complex and challenging nanometer era.



5.2.2 R&D Accomplishments in 2007

R&D Highlights

• 45 Nanometer Technology

2007 was a outstanding year for TSMC's 45nm technology. In the third quarter of 2007, we extended our technology leadership in the foundry sector with qualification and delivery of the first 45nm low-power technology (N45LP) including advanced 193nm immersion lithography, competitive performance-enhancing silicon strains, and extreme low-k inter-metal dielectric material. Our N45LP is believed to have the world's best density and speed at the lowest standby leakage for wireless/RF SoC and handheld applications.

TSMC's leadership in immersion lithography and its success in 45nm technology also paved the road for its successful development of 40nm technology. Both high-performance and low-power 40nm technologies have demonstrated both best-in-class performance and density with good yield. The Company expects to wrap up its development of the 45nm and 40nm technology portfolios in 2008.

As a part of TSMC's shift towards building stronger and tighter foundry-customer co-development relationships for advanced technology, very intensive customer engagement and collaboration were involved throughout the development of both the 45nm and 40nm technologies. This win-win business model was successfully demonstrated as TSMC's new 45nm technology enabled and accelerated customer success. For example, one key TSMC customer successfully placed phone calls using the world's first 45nm 3G cellular phone chip in 2007.

TSMC's 45nm and 40nm technologies extended the Company's industry leadership not only on technical metrics such as performance, power and density, but also in terms of development milestones and customer shuttle verifications. The Company provided its customers with the first-to-market cyber shuttle for both the 45nm and 40nm technologies. First-wave customers have already used more than 200 shuttle blocks.

• 32 Nanometer Technology

In 2007, TSMC led the industry in demonstrating the first 32nm technology, which supported both analog and digital functionalities. The 0.15 μm^2 high-density SRAM cell was realized using 193nm immersion lithography. The full functionality of the 2Mb SRAM test chip was proven with the smallest bit-cell at the 32nm node. This leading-edge technology was optimized for low power, high density and manufacturing margins with optimal process complexity. TSMC plans to provide complete digital, analog and RF functions, as well as high-density memory capabilities at the 32nm node for integrated RF and SoC applications.

TSMC also demonstrated a general-purpose 32nm technology with functional SRAMs intended for high-end ASIC and graphics applications. In addition, the Company has made excellent progress in 32nm high-K/metal gate technology for high performance applications. Early feasibility results were published by TSMC in 2007.

• Immersion Lithography

Immersion lithography provides better depth of focus and enables the industry to continue scaling beyond the 65nm node, all the way to 22nm. It has been more than 5 years since Dr. Burn Lin of TSMC proposed immersion lithography. TSMC was the first to demonstrate 90nm SRAM using the immersion scanner in 2004. The Company was also the first to achieve single-digit immersion-related defects on 300mm wafers in early 2006, demonstrating 65nm customer product chip yield in July 2006. The Company yielded 32Mb SRAM with 45nm process in December 2006, and qualified 45nm at the end of 2007.

TSMC led the industry in achieving manufacturing-ready immersion lithography for the 45nm generation. The Company developed proprietary techniques and resist systems to produce nearly defect-free immersion lithography patterning for volume production.

Overlay performance was also raised to a new level consistent with the requirements of our 45nm and 40nm volume productions, which had the tightest design rules in the industry.

• Long-term Research

2007 was also a great year for TSMC in its expansion of long-term research. One of the technological breakthroughs reported by the NXP-TSMC Research Partnership was a revolutionary embedded memory technology with superior performance, up to 1000 times faster than traditional non-volatile memories, coupled with scalability and reduced power consumption. The estimated power consumption is at least one order of magnitude lower than existing solutions. This technology will be helpful, for example, to prevent data stream interruptions and increase the security of transactions while using near field communication (NFC) to complete mobile payment transactions or content upload.

Another breakthrough was a quartz-replacement resonator for producing smaller and thinner clocks in silicon chips than currently using traditional quartz crystals. This makes it possible to embed clocks into smart cards or SIM cards, which can be used to improve the cryptographic protection of smart cards.

There was also the excellent progress on the next-generation transistor technology in 2007. The research team demonstrated high-performance FinFET devices featuring an optimized gatestack. Another example was the improvement of power consumption in low operational power CMOS devices. Using rapid circuit-based optimization, power consumption was effectively reduced by 80%.

Spectrum of Technologies

Beyond the highlights above, TSMC continued to develop a broad mix of new technologies. The Company accelerated its SoC roadmap, including embedded DRAM (eDRAM) and RF with earlier availability, higher integration and more variants. We are on our way to bring up 45nm RF and eDRAM availabilities by 3 to 6 months after the readiness of the logic platform.

• Embedded DRAM

Embedded DRAM is important for many applications, such as game consoles, digital TVs, networking, base stations, and hard-disk drives. TSMC's eDRAM is fully compatible with the Company's logic technology. In 2007, TSMC qualified 65nm embedded DRAM technologies for both high-speed and low-power applications. These technologies will enter production in early 2008. Several customer products have already been successfully piloted. We also successfully demonstrated 45nm low-power (N45LP) eDRAM and made excellent progress in 40nm general-purpose eDRAM technology.

• Mixed Signal/Radio Frequency (MS/RF) Technology

TSMC completed 65nm MS/RF low-power product qualification in 2007 and successfully moved into production. The technology has enabled one leading cellular phone company to tape out its cellular product with proven SoC functionality. 45nm MS/RF technology was also developed in partnership with early customers. This technology has provided approximately 15% corner tightening for Metal-Oxide-Metal capacitors, an improvement that was also retrofitted to 90nm and 80nm technologies, as well as providing a wide-range inductor

for various design applications. A HVMOS was also developed to fulfill power-management design needs.

• Silicon Germanium BiCMOS Technology

Through intensive yield improvement efforts, TSMC's silicon germanium (SiGe) BiCMOS technology achieved the same yield level as its MS/RF CMOS technology. Combined with the Through-Silicon-Via (TSV) technology developed in 2007, TSMC's SiGe BiCMOS technology can now provide a high-performance, cost-effective solution to power amplifier applications, enabling a higher level of design integration. A variety of passive devices were also developed, including a high-density ($2.0\text{fF}/\mu\text{m}^2$) metal-insulator-metal (MiM) capacitor, 46KA ultra-thick-metal, and a linear poly/sinker capacitor, for cost-effective yet high-performance MS/RF design.

• CMOS Image Sensor Technology

A high-performance, low-cost $0.11\mu\text{m}$ 4T CMOS image sensor (CIS) process with aluminum-copper backend was successfully developed and qualified by TSMC in 2007. This new process aimed at high-end imaging applications with a small pixel size of $1.75\mu\text{m}$ and high resolutions of greater than three megapixels. It was compatible with TSMC's $0.13\mu\text{m}$ CMOS logic, which enabled SoC platforms in mobile phones, digital cameras, security sensors, automotive applications and other image sensor markets. Color backside illumination image capability was also successfully demonstrated. This can extend $0.11\mu\text{m}$ CIS technology to smaller pixel sizes ($1.4\mu\text{m}$) and ultra-high resolutions (larger than eight megapixels).

• Flash/Embedded Flash Technology

In 2007, TSMC also completed the qualification of its automotive-grade application using embedded flash (embFlash) processes at the $0.18\mu\text{m}$ technology node. Production is well underway. In addition, $0.13\mu\text{m}$ embFlash technology was also qualified for commercial embFlash prototype activities. For next-generation embFlash technology, a new cell with scaling capabilities of the 90nm and 65nm nodes was demonstrated. A test vehicle with 32Mb flash IP has been proven with good yield.

• Mask Technology

Mask technology is an integral part of advanced lithography. TSMC has developed proprietary resolution-enhancement techniques that were highly optimized with our in-house mask-making technology, including optical proximity correction (OPC), subresolution-assist mask features, and phase-shifting masks. In 2007, we implemented a low-cost, high-precision OPC methodology based on our proprietary hardware and software approaches. Our OPC methodology significantly improved the cycle time, while maintaining the high accuracy required for both the 45nm and 32nm technology nodes. Fast Lithography Process Check (LPC) technology and Design For Manufacturing (DFM) were also being extended to the 45nm node. TSMC mask facilities featured state-of-the-art E-beam mask writers, etchers, and inspection and repair tools for both R&D and production usages at 45nm, and were moving steadily towards 32nm. TSMC's strength in mask technology provides significant benefits to our customers in terms of technical excellence, quality, fast cycle time, and one-stop service.

5.2.3 Intellectual Property

A strong portfolio of intellectual property strengthens TSMC's technology leadership. In 2007, TSMC received 462 U.S. patents, 322 Taiwanese patents, 111 PRC patents, and other patents issued in countries around the world. We are in the process of implementing a unified model for TSMC's intellectual capital management. Strategic considerations and close alignment with business objectives now drive the creation, management and use of our intellectual property.

At TSMC, we have built a process to extract value from our intellectual property by aligning our intellectual property strategy with our R&D, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities.

We have worked continuously to improve the quality of our intellectual property portfolio and to reduce the cost of maintaining it. We expect to continue investing in our intellectual property portfolio and intellectual property management system to ensure that we receive maximum business value from our intellectual property rights.

5.2.4 Future R&D Plans

In 2008, TSMC plans to focus on the development and qualification of the 32nm logic/mixed signal technology platforms as well as the exploratory study of a 22nm logic technology platform. Both nodes should have superior transistor performance, high-k dielectric and metal gate processes. Other development projects will include 45nm embedded DRAM; 45nm/40nm mixed signal/RF for communications applications; embedded flash IP development in 90nm/65nm technologies; and 90nm CMOS image sensor technology.

Following the significant successes of TSMC's advanced technologies in 2007, the Company plans to continue to grow the R&D organization. TSMC will further expand the 300mm R&D pilot line to speed up 32nm qualification with its early engagement customers and the 22nm exploratory research programs with world-leading research institutions. We plan to reinforce our exploratory development work on new transistors and technologies such as 3D structures, MRAM, strained-layer CMOS, and novel 3D-IC devices with TSV. The study of the fundamental physics of nanometer CMOS transistors is a core aspect of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to ensure our continued industry leadership at the 32nm and 22nm nodes. One of TSMC's goals is to extend Moore's law through innovative in-house work, as well as by collaborating with industry leaders and academia to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC plans to continue working closely with international consortia and photolithography equipment suppliers to ensure the timely development of 193nm high-NA scanner technology, liquid immersion lithography, EUV lithography, and massively parallel E-

Beam direct-write technologies. These technologies are now fundamental to our process development efforts at the 32nm and 22nm nodes and beyond.

TSMC plans to continue its collaboration with mask inspection equipment suppliers to develop viable inspection techniques. This collaborative partnership should help to ensure that we maintain our leadership position in mask quality and cycle time, and continue to meet aggressive R&D, prototyping and production requirements.

Overall, TSMC will continue to invest heavily to expand our R&D capabilities. With a highly competent and dedicated R&D team and unwavering commitment to innovation, we are confident of our ability to deliver the best and most cost-effective SoC technologies for our customers, and to support our business growth and profitability.

TSMC R&D future major project summary:

Project Name	Description	Risk Production (Estimated Target Dates)
40nm logic platform technology and applications	40nm general-purpose and low-power SoC technologies with embedded memory and analog/RF	2008
32nm logic platform technology and applications	Next-generation technology for both digital and analog products	2009
22nm logic platform technology and applications	Exploratory technology for both digital and analog products	2011
3D-IC	Low cost solution with better form factor and performance for SIP	2010-2011
Next-generation lithography	EUV and multiple E-Beam to extend Moore's Law	2011-2012
Long-term research	Special SoC technology (including new NVM, MEMS, RF, analog) and 15nm transistors	2012-2014
The above plans account for roughly 70% of total corporate R&D budget in 2008.		

5.3 Manufacturing Excellence

5.3.1 Efficiency

Fast Yield Ramp Up

Fast yield ramp for new products is a key factor behind the success of TSMC and its customers. The Company has developed a comprehensive technology transfer methodology extending from R&D to production in order to shorten new technology learning curve. TSMC's seamless technology transfer also enables consistent yields when customers transfer production to a second internal fab. In 2007, the Company delivered a significant breakthrough on 65nm ramp-up by shortening the yield learning curve by 20% in comparison with that of the previous generation, 90nm.

Accurate Delivery

TSMC has a proven record of providing customers with consistent on-time delivery. To become even more responsive to our customers' need for flexibility in delivery, TSMC has re-engineered its demand fulfillment system with a state-of-the-art manufacturing scheduling system. The system further enhances the accuracy of our deliveries to our customers.

Best-in-Class Cycle Time Management

One of the keys to our customer's success is TSMC's ability to deliver products with short demand fulfillment cycle times. To achieve this for our customers, TSMC has developed a sophisticated manufacturing scheduling and dispatching system, implemented industry-leading automated materials handling systems, and employed effective lean manufacturing approaches. TSMC strives unceasingly to improve the productivity of both people and equipment, and its cycle times are among the best in the semiconductor industry.

Flexible Manufacturing Management

Flexible Manufacturing is a crucial element that addresses the fluctuations in demand forecast. In most cases, TSMC has the ability to meet unanticipated customer demand surges, thanks in large part to our cluster fab capability as well as extensive know-how in performance matching for both tools and Fabs.

Knowledge Management

TSMC has built the industry's leading, state-of-the-art knowledge management, and Best Known Method (BKM) systems. TSMC maintains a vast repository system for key knowledge. This database also features a sophisticated expert system that embeds the captured knowledge into TSMC's engineering system.

Inventory Management

TSMC made continuous improvements in materials and inventory management in 2007. Demand and supply information from the materials management and other related departments was integrated using a system of real-time updates and reports. The system is intended to improve the Company's responsiveness to wafer demand forecasts. The speed and accuracy of TSMC's response has been improved through real-time demand information sharing. This ensures that the Company can continue to appropriately respond to ever-changing industry conditions.

5.3.2 GigaFab™

TSMC's 12-inch fabs are a key part of its manufacturing strategy. TSMC currently operates two 12-inch GigaFabs™ — Fab 12 and Fab 14. The combined capacity of the two GigaFabs™ reached 388,000 12-inch wafers or 873,000 8-inch equivalent wafers in the fourth quarter of 2007. Production within these two facilities supports 0.13μm, 90nm, 65nm and 45nm process technologies. Part of the capacity is reserved for research and development work and currently supports 32nm and beyond technology development.

These GigaFabs™ are the center stones of TSMC's unceasing efforts to improve manufacturing excellence and to deliver manufacturing breakthroughs. Not only do these GigaFabs™ have the inherent scale advantages over smaller fabs, they also enable greater flexibility to adapt to demand fluctuations, improve product quality and yields, accelerate yield learning and time to volume, shorten cycle times, and minimize costly product re-qualification.